L Number	Hits	Search Text	DB	Time stamp
1	20	SONET$ same LVDS	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 17:45
2	10	((synchronous ADJ digital adj hierarchy) or SDH) same lvds	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 17:47
3	608	8b/10b	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 17:47
4	66	sonet same 8b/10b	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:44
5	6	lvds and (sonet same 8b/10b)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 19:00
6	1	370/$.ccls. and 710/$.ccls. and lvds and (sonet$ or sdh)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 19:03
7	35	370/$.ccls. and lvds and (sonet$ or sdh)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 19:15
8	4	8b/10b and (370/$.ccls. and lvds and (sonet$ or sdh))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 19:15

09/847,660

Your search matched **0** of **1003743** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.

sbi336s Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

Results:
No documents matched your query.

h eee e eee g e ch e ch e e b c e e c

Google Advanced Search Preferences Language Tools Search Tips

SBI336S Google Search

Web · Images · Groups · Directory · News

Searched the web for SBI336S. Results 1 - 4 of about 12. Search took 0.13 seconds.

Tip: In most browsers you can just hit the return key instead of clicking on the search button.

PMC-Sierra > PM8610 SBS TelecomBus or SBI bus bridge, STS-12 Time ...
... and implements bridging or conversion between byte-serial 77.76MHz SBI336 bus or Telecom Bus and redundant 777.6Mbps bit-serial 8B/10B-base **SBI336S** bus or ...
www.pmc-sierra.com/products/details/pm8610/ - 49k - Cached - Similar pages

PMC-Sierra > PM8621 NSE 8G - 12x12 crossbar switch, each input and ...
... links. Each port can be either Serial TelecomBus or Serial **SBI336S**. ... links. Each port can be either Serial TelecomBus or Serial **SBI336S**. ...
www.pmc-sierra.com/products/details/pm8621/ - 42k - Cached - Similar pages
[More results from www.pmc-sierra.com]

[PDF] PM8610 SBI Bus Serializer / STS-12 Time Slot Interchange Short ...
File Format: PDF/Adobe Acrobat - View as HTML
... circuit that implements conversion between byte- serial 19.44Mhz SBI bus or 77.76MHz SBI336 bus and redundant 777.6Mbps bit-serial 8B/10B-base **SBI336S** bus. ...
www.memec-impact.ch/pdf/pmc/PM8610DataSheet.pdf - Supplemental Result - Similar pages

[PDF] Narrowband Switch Element 20G (NSE-20G) Standard Product Data ...
File Format: PDF/Adobe Acrobat - View as HTML
... 45 9.3 Transmit 8B/10B Encoder (T8TE)....45 9.3.1 **SBI336S** 8B/10B Character Encoding ...
www.memec-impact.ch/pdf/pmc/PM8620DataSheet.pdf - Supplemental Result - Similar pages
[More results from www.memec-impact.ch]

In order to show you the most relevant results, we have omitted some entries very similar to the 4 already displayed.
If you like, you can repeat the search with the omitted results included.

SBI336S Google Search Search within results

Dissatisfied with your search results? Help us improve.

Get the Google Toolbar: Google Search Web PageRank 6 blocked AutoFill

Google Home - Advertise with Us - Business Solutions - Services & Tools - Jobs, Press, & Help

h g gec e ch h e e e b g e e ch

Your search matched **1** of **1003743** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.

8b/10b<and>sdh Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Transparent generic framing procedure (GFP): a protocol for efficient transport of block-coded data through SONET/SDH networks**
Gorshe, S.S.; Wilson, T.;
Communications Magazine, IEEE , Volume: 40 , Issue: 5 , May 2002
Pages:88 - 95

[Abstract] [PDF Full-Text (547 KB)] **IEEE JNL**

---

h eee e eee g e ch e ch e e c e e e c e

Your search matched **1** of **1003743** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.

lvds<and>sdh Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Low-power fully integrated 10-Gb/s SONET/SDH transceiver in 0.13-/spl mu/m CMOS**
Henrickson, L.; Shen, D.; Nellore, U.; Ellis, A.; Joong Oh; Hui Wang; Capriglione, G.; Atesoglu, A.; Yang, A.; Wu, P.; Quadri, S.; Crosbie, D.;
Solid-State Circuits, IEEE Journal of , Volume: 38 , Issue: 10 , Oct. 2003
Pages:1595 - 1601

[Abstract] [PDF Full-Text (479 KB)] **IEEE JNL**

---

h eee e eee g e ch e ch e e c e e e c e

Your search matched **4** of **1003743** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.

lvds<and>sonet Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **OC-192 transmitter and receiver in standard 0.18-/spl mu/m CMOS**
Cao, J.; Green, M.; Momtaz, A.; Vakilian, K.; Chung, D.; Keh-Chee Jen; Caresosa, M.; Wang, X.; Wee-Guan Tan; Yijun Cai; Fujimori, L.; Hairapetian, A.;
Solid-State Circuits, IEEE Journal of , Volume: 37 , Issue: 12 , Dec. 2002
Pages:1768 - 1780

[Abstract] [PDF Full-Text (1087 KB)] **IEEE JNL**

---

2 **OC-192 receiver in standard 0.18µm CMOS**
Jun Cao; Momtaz, A.; Vakilian, K.; Green, M.; Chung, D.; Keh-Chee Jen; Caresosa, M.; Ben Tan; Fujimori, I.; Hairapetian, A.;
Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International , Volume: 1 , 3-7 Feb. 2002
Pages:250 - 464 vol.1

[Abstract] [PDF Full-Text (411 KB)] **IEEE CNF**

---

3 **Fully-integrated SONET OC48 transceiver in standard CMOS**
Momtaz, A.; Cao, J.; Caresosa, M.; Hairapitian, A.; Chung, D.; Vakitian, K.; Green, M.; Tan, B.; Keh-Chee Jen; Fujimori, I.; Gutierrez, G.; Yijun Cai;
Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International , 5-7 Feb. 2001
Pages:76 - 77, 433

[Abstract] [PDF Full-Text (208 KB)] **IEEE CNF**

---

4 **Low-p wer fully integrated 10-Gb/s SONET/SDH transceiver in 0.13-/spl mu/m CMOS**
Henrickson, L.; Shen, D.; Nellore, U.; Ellis, A.; Joong Oh; Hui Wang; Capriglione, G.; Atesoglu, A.; Yang, A.; Wu, P.; Quadri, S.; Crosbie, D.;

h eee e eee g e ch e ch e e c e e e c e

Solid-State Circuits, IEEE Journal of , Volume: 38 , Issue: 10 , Oct. 2003
Pages:1595 - 1601

[Abstract] [PDF Full-Text (479 KB)] **IEEE JNL**

h eee e eee g e ch e ch e e c e e e c e

Your search matched **2** of **1003743** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.

8b/10b<and>sonet Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **Transparent generic framing procedure (GFP): a protocol for efficient transport of block-coded data through SONET/SDH networks**
Gorshe, S.S.; Wilson, T.;
Communications Magazine, IEEE , Volume: 40 , Issue: 5 , May 2002
Pages:88 - 95

[Abstract] [PDF Full-Text (547 KB)] **IEEE JNL**

2 **SiGe BiCMOS 3.3-V clock and data recovery circuits for 10-Gb/s serial transmission systems**
Meghelli, M.; Parker, B.; Ainspan, H.; Soyuer, M.;
Solid-State Circuits, IEEE Journal of , Volume: 35 , Issue: 12 , Dec. 2000
Pages:1992 - 1995

[Abstract] [PDF Full-Text (76 KB)] **IEEE JNL**

h eee e eee g e ch e ch e e c e e e c e

Your search matched **2** of **1003743** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.

8b/10b<and>encoding Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **AC-coupled burst-mode optical receiver employing 8B/10B coding**
Han, S.; Lee, M.S.;
Electronics Letters , Volume: 39 , Issue: 21 , 16 Oct. 2003
Pages:1527 - 1528

[Abstract] [PDF Full-Text (197 KB)] **IEE JNL**

---

2 **The simple link protocol: a zero-overhead packet delineation scheme for high-speed Ethernet**
Truman, T.E.; Leilei Song; Azadet, K.;
VLSI Technology, Systems, and Applications, 2001. Proceedings of Technical Papers. 2001 International Symposium on , 18-20 April 2001
Pages:65 - 68

[Abstract] [PDF Full-Text (348 KB)] **IEEE CNF**

---

h eee e eee g e ch e ch e e c e e e c e

PGPUB-DOCUMENT-NUMBER: 20020001305

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020001305 A1

TITLE: Flexible, self-aligning time and space switch fabrics

PUBLICATION-DATE: January 3, 2002

related
2 have same inventor

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
RULE-47			
Hughes, Andrew Milton	Saskatoon		CA
Konkin, Douglas	Saskatoon		CA
McCrosky, Carl Dietz	Saskatoon		CA
Mok, Winston	Vancouver		CA
Roe, Jeffrey Scott	Saskatoon		CA
Sailor, Kenneth Evert	Saskatoon		CA

US-CL-CURRENT: 370/369, 370/442

ABSTRACT:

A time:space:time switch fabric incorporating an odd integer number of spatially distributed data switches and a plurality of spatially distributed data serializers. Each data switch has a first plurality of ingress ports, an equal plurality of egress ports, and a space switch for selectably interconnecting any one of the ingress ports to any one of the egress ports. Each data serializer has an input bus for receiving signals to be routed through the switch fabric, an output bus for outputting signals routed through the switch fabric, a plurality of egress ports selectably connectible to any one of the data switch ingress ports, and an equal plurality of ingress ports selectably connectible to any one of the data switch egress ports. The ingress/egress ports are characterized by:
(A) p planes, where p is a power-of-two integer less than or equal to the number of data serializer ingress and egress ports;
(B) s stages, where s is an odd integer number; and,
(C) a depth d, where d is a power-of-two integer less than or equal to the number of data switch ingress and egress ports.

---------- KWIC ---------

Detail Description Paragraph - DETX (4):
[0044] A significant aspect of the invention is the use of fast serial links to transport signals to and from the ports on the TSEs and TBSs which comprise any given fabric. Fast, constant current **LVDS** (low-voltage differential signaling) at 777.6 Mb/s is used to carry each STS-12 signal. This speed is dependent on the details of the **SONET** standards, but the essential issues involved in this invention's use of serial link technology are independent of **SONET**. Nevertheless, particulars of the **SONET** implementation are provided to assist persons skilled in the art in comprehending the invention.

PGPUB-DOCUMENT-NUMBER: 20010056512

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010056512 A1

TITLE: Bus interface for transfer of SONET/SDH data

PUBLICATION-DATE: December 27, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
RULE-47			
Mok, Winston K.	Vancouver		CA
Lang, Steven F.	Vancouver		CA
McCrosky, Carl D.	Saskatoon		CA
Tse, Richard T.	Vancouver		CA

US-CL-CURRENT: 710/100

ABSTRACT:

This invention provides a bus interface to connect SONET/SDH termination devices with payload processing devices while utilizing a minimum number of signals. The bus interface of this invention can scale with future advances in bandwidth in serial link technology.

---------- KWIC ---------

Summary of Invention Paragraph - BSTX (12):

[0010] The method consists of providing a transmit interface and a receive interface. In operation, the transmit interface receives an incoming **SONET/SDH** signal stream and converts the **SONET/SDH** signal stream into outgoing low voltage differential signal (**LVDS**) levels. The **SONET/SDH** signal streams are mapped into 8B/10B control characters to label the **SONET/SDH** frame boundaries. Potential **SONET/SDH** frame boundaries include transport frame, high-order path frame and low-order path frame boundaries.

Summary of Invention Paragraph - BSTX (13):

[0011] The receive interface receives incoming **LVDS** signal levels and converts the **LVDS** levels into and outgoing **SONET/SDH** signal streams. The 8B/10B control characters labeling the **SONET/SDH** frame boundaries are decoded into **SONET/SDH** control signals.

Claims Text - CLTX (2):

1. A method of connecting **SONET/SDH** termination devices with payload processing devices, comprising: (a) providing a transmit interface operative to receive incoming **SONET/SDH** signal streams and convert said **SONET/SDH** signal streams into outgoing low voltage differential signal (**LVDS**) levels with said **SONET/SDH** signal streams mapped into 8B/10B control characters so as to label **SONET/SDH** frame boundaries; and (b) providing a receive interface operative to receive incoming **LVDS** signal levels and convert said **LVDS** signal levels into outgoing **SONET/SDH** signal streams with decoding of said sB/10B control characters labeling **SONET/SDH** frame boundaries into **SONET/SDH** control signals.

Claims Text - CLTX (12):

11. A bus interface device for connecting **SONET/SDH** termination devices with payload processing devices, comprising: (a) a transmit interface operative to receive incoming **SONET/SDH** signal streams and convert said **SONET/SDH** signal streams into outgoing low voltage differential signal (**LVDS**) levels with said **SONET/SDH** signal streams mapped into 8B/10B control characters so as to label **SONET/SDH** frame boundaries; and (b) a receive interface operative to receive incoming **LVDS** signal levels and convert said **LVDS** signal levels into outgoing **SONET/SDH** signal streams with decoding of said 8B/10B control characters labeling **SONET/SDH** frame boundaries into **SONET/SDH** control signals.

US-PAT-NO: 6381269

DOCUMENT-IDENTIFIER: US 6381269 B1

TITLE: Test system with signal injection network for characterizing interference and noise tolerance in a digital signal link

DATE-ISSUED: April 30, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gradl; David A.	Naperville	IL	N/A	N/A
Steinberger; Michael L.	Woodenville	WA	N/A	N/A

US-CL-CURRENT: 375/224, 324/520 , 324/521 , 324/527 , 714/715

ABSTRACT:

A test system for a evaluating a digital signal link includes a data signal generator, a data signal receiver, a digital signal link to be tested and a test interference signal injection (TISI) network connected as part of the digital signal link. The TISI network includes a data signal input port for receiving digital data signals generated by the data signal generator, a data signal output port for providing the digital data signals to the data signal receiver, and a controlled impedance data signal path carrying the digital data signals between the data signal input port and the data signal output port. An interference signal input port receives interference signals over a range of frequencies from an interference signal generator. One or more directional couplers directionally couple the interference signals into the data signal path toward either the data signal output port or the data signal input port at an impedance that substantially matches the impedance of the digital signal link. The directional couplers are configured to maintain d.c. isolation from ground to facilitate the transfer of d.c. coupled data signal logic through the TISI network.

20 Claims, 13 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 13

---------- KWIC ---------

Detailed Description Text - DETX (2):

Turning now to the figures, wherein like reference numerals represent like elements in all of the several views, FIG. 1 illustrates a test system 1 for testing a digital signal link 2 for interference tolerance. A test interference signal injection (TISI) network 4 is connected as part of the digital signal link 2 in order to introduce interference signals therein. The digital signal link 2 is configured, by way of example only, as a low voltage digital signal (**LVDS**) serial data link operating at a data transfer rate of 622 Mbps to simulate high speed asynchronous transfer mode (ATM) or synchronous optical network (**SONET**) transmissions, or communications based on any other applicable protocol. The digital signal link 2 is connected in the test system 1 to receive a pseudo random bit pattern data signal from a bit error rate (BER) pattern generator 6 and to carry that signal to a BER receiver 8. By way of example only, a model HP70841B.TM. BER pattern generator could be used to

implement the BER pattern generator 6 and a model HP70842B.TM. BER receiver could be used to implement the BER receiver 8. The pattern generator 6 in the embodiment of FIG. 1 produces emitter coupled logic (ECL) voltage level data signals. These ECL logic levels are translated to LVDS levels by an ECL-LVDS translation buffer 10, and fed to an LVDS driver 12 that amplifies the LVDS data signals and matches the output impedance to a standard line impedance of 50 ohms. The LVDS data signals are passed through an integrated circuit (IC) socket 14 to a first connector 16 which, by way of example only, could be a METRAL.TM. brand 5.times.6 pin header-receptacle pair.

Detailed Description Text - DETX (11):

The outbound and inbound digital signal links 41a and 41b are implemented in the embodiment of FIG. 2 as high speed serial data link carrying 622 Mbps LVDS serial data signals to simulate inter-IC and inter-PWB communications based on ATM, SONET or any other applicable protocol. The outbound digital signal link 41a extends from the test board 42 to the UUT 50 along a high speed serial communication link segment 54. The inbound digital signal link 41b extends from the UUT 50 to the test board 42 along a link segment 56. The link segments 54 and 56 respectively connect to receiver end and driver end circuits 57 and 58 in the UUT 50. The link segments 54 and 56 could be implemented using any suitable data transmission media, such as shielded cabling (using two cables per segment) or the like. The UUT 50 itself could be any digital signal processing unit having respective receive-side and transmit-side components 57 and 58. In addition, as described in more detail below, the UUT 50 typically have a loop-back mode that allows digital signals input to the receiver end 57 to be returned via the driver end 58 while bypassing the normal signal processing components of the UUT 50.

US-PAT-NO: 6359859

DOCUMENT-IDENTIFIER: US 6359859 B1

TITLE: Architecture for a hybrid STM/ATM add-drop multiplexer

DATE-ISSUED: March 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Brolin; Stephen J.	Livingston	NJ	N/A	N/A
DeMarco; Robert W.	Whippany	NJ	N/A	N/A

US-CL-CURRENT: 370/218, 370/352 , 370/395.1 , 370/401 , 370/407 , 370/425 , 709/201 , 709/221 , 709/249 , 709/252

ABSTRACT:

An architecture for a SONET network element, such as a hybrid STM/ATM add-drop multiplexer. The disclosed system includes an interconnection system for a network element, including a line unit slot, a switch fabric slot, and two or more service unit slots. The line unit slot is connected as a hub to the switch fabric slot and the service unit slots in a first star interconnection configuration. The switch fabric slot is connected as a hub to the line unit slot and the service unit slots in a second star interconnection configuration. The star interconnection configurations provide fault isolation between different units, and allow for replacement of failed units without interfering with the links of other units to the hub. In a preferred embodiment, the switch fabric slot and one of the service unit slots comprise the same slot, thus permitting flexible configuration of the device within a minimal space. In a further illustrative embodiment, a control unit slot is provided in the interconnection system, and connected as a hub to the line unit slot, the switch fabric slot, and the service unit slots to form a third star interconnection configuration. A service unit is also disclosed, including a first backplane interface for connecting with an ATM star interconnect configuration within the network element, and a second backplane interface for connecting to an STM star interconnect configuration within said network element. The service unit further includes a third backplane interface to connect with a control star interconnect configuration within the network element.

28 Claims, 17 Drawing figures

Exemplary Claim Number: 13

Number of Drawing Sheets: 17

---------- KWIC ---------

Brief Summary Text - BSTX (33):

Thus there is provided a communication device which combines the functions of a **SONET** add-drop multiplexer with the functions of an ATM switch. The disclosed device supports multiple configurations, including STM only, ATM only, or hybrid STM/ATM operation. Moreover, the disclosed device is flexible and scalable such that functionality may be added or modified as the needs of the customer change over time. The disclosed system advantageously applies low voltage, complementary signaling techniques such as Low Voltage Differential Signaling (**LVDS**) to provide high speed, serial point to point links in star

configurations. The use of serial point to point links supports failure isolation, since failure of a single non-hub unit will not affect the connections of other units to the hub of the star. Accordingly, replacement of a non-hub unit is possible without disturbing the operation of the other units in the star. The disclosed system supports failure protection in hub units, such as the line units and ATM switch fabric units, by providing connectivity for active/standby unit pairs of the line unit and ATM switch fabric unit. In addition, by use of multi-function service unit slots, which can also serve as ATM switch fabric unit slots, the disclosed system supports a wide variety of configurations in a minimum amount of space.

Detailed Description Text - DETX (34):

FIG. 7 is a functional block diagram of an illustrative line unit 100. The line unit 100 provides an optical interface to a SONET ring at the line side of the disclosed network element. The line unit 100 is shown including a signal routing ASIC 102, which is coupled to an optical receiver 104, an optical transmitter 106, ATMU Low Voltage Differential Signaling (LVDS) receivers 108, ATMU transmitters 110, and an STM switch fabric ASIC 114. ATMU transmitters 110 and ATMU receivers 108 are, for example, shown using LVDS devices. The STM switch fabric ASIC 114 is shown including service unit transmit interfaces 116 and service unit receive interfaces 118.

US-PAT-NO: 6317439

DOCUMENT-IDENTIFIER: US 6317439 B1

TITLE: Architecture for a SONET line unit including optical transceiver, cross-connect and synchronization subsystem

DATE-ISSUED: November 13, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Cardona; Gabriel E.	Garland	TX	N/A	N/A
Honaker, Jr.; Charles M.	Garland	TX	N/A	N/A
Baydar; Ertugrul	Grapevine	TX	N/A	N/A

US-CL-CURRENT: 370/503, 370/324 , 370/350

ABSTRACT:

A SONET interface line unit which includes an interface to a SONET ring, an STM switch fabric, and STM synchronization function within a single module. The line unit includes an optical interface for communicating SONET traffic with a SONET ring, an ATM interface for communicating ATM traffic with an ATM switch fabric unit, and two or more service unit interfaces for communicating with service units having service interfaces to a service side of a network element. The service unit interfaces operate using the STM protocol. The line unit further includes forwarding logic for extracting ATM traffic and STM traffic from the composite traffic received from the SONET ring. The line unit further provides synchronization signals to other units within the network element, derived from a selected timing reference signal. An extended synchronization module is used to interface to a larger number of timing references within the device.

15 Claims, 17 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 17

---------- KWIC ---------

Detailed Description Text - DETX (34):

FIG. 7 is a functional block diagram of an illustrative line unit 100. The line unit 100 provides an optical interface to a **SONET** ring at the line side of the disclosed network element. The line unit 100 is shown including a signal routing ASIC 102, which is coupled to an optical receiver 104, an optical transmitter 106, ATMU Low Voltage Differential Signaling (**LVDS**) receivers 108, ATMU transmitters 110, and an STM switch fabric ASIC 114. ATMU transmitters 110 and ATMU receivers 108 are, for example, shown using **LVDS** devices. The STM switch fabric ASIC 114 is shown including service unit transmit interfaces 116 and service unit receive interfaces 118.

PGPUB-DOCUMENT-NUMBER: 20010014104

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010014104 A1

TITLE: 10 Gigabit ethernet mappings for a common LAN/WAN PMD interface with a simple universal physical medium dependent interface

PUBLICATION-DATE: August 16, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
RULE-47			
Bottorff, Paul A.	Palo Alto	CA	US
Figueira, Norival R.	San Jose	CA	US
Martin, David W.	Stittsville		CA
Armstrong, Timothy J.	Stittsville		CA
Raahemi, Bijan	Nepean		CA

US-CL-CURRENT: 370/471, 370/419 , 370/474 , 370/477 , 370/537 , 370/543

ABSTRACT:

An Ethernet mapping enables high speed Ethernet data streams having a data rate of 10 Gb/s to be transported across a synchronous packet switched network fabric having a standard SONET OC-192 line rate of 9.953280 Gbaud. The 10 Gb/s Ethernet data stream is compressed by removing interframe gaps between successive MAC frames to produce a compressed data stream, which is then mapped to a synchronous container. The synchronous container is then launched across the synchronous packet switched network fabric at a standard SONET OC-192 line rate of 9.953280 Gbaud. The synchronous container is preferably provided as a stripped STS-192c frame having only A1 and A2 octets of the Transport Overhead (TOH). The compressed data stream is mapped directly to the synchronous container, starting at the first octet following the A1 and A2 octets, without first being inserted into a conventional STS-192c SPE, so that most of the space normally used for TOH and Path overhead (POH) within a conventional STS-192c frame is freed-up for carrying the compressed data stream. At a receiving interface, the compressed data stream is extracted from received synchronous containers and decompressed, by insertion of interframe gaps between successive MAC frames, to generate a recovered 10 Gb/s Ethernet data stream. The starting bit of each successive MAC frame can be identified by examination of the length field of the immediately previous MAC frame.

---------- KWIC ---------

Detail Description Paragraph - DETX (8):

[0034] FIG. 2 schematically shows a prior art physical layer interface for coupling high speed Ethernet traffic to a **SONET**/SDH packet switched network medium 4. As shown in FIG. 2, the conventional PCS 10 and PMA 12 are grouped together as a combined PCS/PMA HARI 30 which mediates data transport between the (conventional) data link layer 8 and a modified PMD sub-layer 14a. The HARI 30 exchanges data with the modified PMD 14a using 4 parallel data channels (in each direction) operating at a line rate of 3.125 Gbaud. The modified PMD 14a is subdivided into **8B/10B** and 64/66 encoding layers 32,34; a framer FIFO 36; a scrambler 38; and a conventional electron/optical conversion layer 40.

Thus in the prior art device of FIG. 2, much of the data encoding, framing, and scrambling functionality conventionally performed in the PCS 10 and PMA 12 are relocated into the PMD 14a. The PMD 14a is designed to operate in one of two modes depending on the LAN/WAN configuration of the network (see FIG. 7). In particular, in a LAN configuration, this interface is intended to achieve a data rate in the data link layer 8 of 10 Gb/s, in conformance with the high speed Ethernet standard. In order to obtain this data rate, the framer FIFO 36, scrambler 38 and converter 40 of the PMD 14a (and medium 4) is operated at a line rate of 10.3125 Gbaud. This line rate is significantly higher than that supported by the SONET/SDH standard, which precludes the use of conventional (and legacy) SONET/SDH routing systems within the network medium 4.

PGPUB-DOCUMENT-NUMBER: 20020001305

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020001305 A1

TITLE: Flexible, self-aligning time and space switch fabrics

PUBLICATION-DATE: January 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
RULE-47			
Hughes, Andrew Milton	Saskatoon		CA
Konkin, Douglas	Saskatoon		CA
McCrosky, Carl Dietz	Saskatoon		CA
Mok, Winston	Vancouver		CA
Roe, Jeffrey Scott	Saskatoon		CA
Sailor, Kenneth Evert	Saskatoon		CA

US-CL-CURRENT: 370/369, 370/442

ABSTRACT:

A time:space:time switch fabric incorporating an odd integer number of spatially distributed data switches and a plurality of spatially distributed data serializers. Each data switch has a first plurality of ingress ports, an equal plurality of egress ports, and a space switch for selectably interconnecting any one of the ingress ports to any one of the egress ports. Each data serializer has an input bus for receiving signals to be routed through the switch fabric, an output bus for outputting signals routed through the switch fabric, a plurality of egress ports selectably connectible to any one of the data switch ingress ports, and an equal plurality of ingress ports selectably connectible to any one of the data switch egress ports. The ingress/egress ports are characterized by:
(A) p planes, where p is a power-of-two integer less than or equal to the number of data serializer ingress and egress ports;
(B) s stages, where s is an odd integer number; and,
(C) a depth d, where d is a power-of-two integer less than or equal to the number of data switch ingress and egress ports.

---------- KWIC ---------

Brief Description of Drawings Paragraph - DRTX (2):
[0025] FIG. 1 schematically depicts a transmission switching element (TSE) having 64 low voltage differential signal (**LVDS**) ports.

Brief Description of Drawings Paragraph - DRTX (3):
[0026] FIG. 2 schematically depicts a telecommunications bus serializer (TBS) having four "working" **LVDS** ports, four "protection" **LVDS** ports, and four "auxiliary" **LVDS** ports.

Detail Description Paragraph - DETX (4):
[0044] A significant aspect of the invention is the use of fast serial links

to transport signals to and from the ports on the TSEs and TBSs which comprise any given fabric. Fast, constant current **LVDS** (low-voltage differential signaling) at 777.6 Mb/s is used to carry each STS-12 signal. This speed is dependent on the details of the SONET standards, but the essential issues involved in this invention's use of serial link technology are independent of SONET. Nevertheless, particulars of the SONET implementation are provided to assist persons skilled in the art in comprehending the invention.

Detail Description Paragraph - DETX (6):

[0046] Fast serial link receivers (such as, but not limited to, **LVDS**) must address a fundamental problem: they must be able to recover the clock of the transmitted signal in order to recover and properly time the transmitted data. Clock is not transmitted, but is recovered by observing the transitions present (0 to 1 and 1 to 0) in the transmitted data. It is possible for the transmitter to transmit a long series of bits without transitions, depending on users' traffic patterns and on encapsulating protocols designed into the system. Such transitionless sequences could lead to loss of clocking at the receiver. There are two standard approaches to avoiding this problem: the use of an expanded code (e.g. 8b/10b) to allow the basic eight bit codes to be embedded in a larger code space (e.g. the 10 bit code space of 8b/10b) in such a way as to avoid transmitting code words which contain too few transitions. The present invention adopts 8b/10b coding to obtain adequate transitions at the receiver to recover the transmitter's clock. The serial bit stream carrying 8b/10b codes must be properly framed into its 10b code words. This is done by examining the bit stream at each possible code word alignment (there are ten), until an alignment is found which generates no line code violations. This is standard practice.

Detail Description Paragraph - DETX (7):

[0047] As previously explained, time and space fabrics must allow all switching stages to recognize and coordinate their switching activities to the boundaries of the grain groups. The present invention uses a special code of **8b/10b** to mark the beginnings of STS-1 frame boundaries. The **8b/10b** "comma" character is used to mark at least some of the beginnings of STS-1 frames (in the **SONET** J0 octet). This allows the receivers of the TSE and the TBS to recognize STS-1 frame boundaries. The **SONET** frame boundary is used to reset a counter which counts through the repeating 12*9*90 octets of the STS-12 frame. This counter, reduced modulo-twelve, is used to identify the relative positions of the grains of the twelve STS-1s.

Detail Description Paragraph - DETX (8):

[0048] The **8b/10b** "comma" special character is not required to be present in each **SONET** frame; the first occurrence of the comma character sets the frame counter, which then runs modulo-(12*9*90) to count out the positions in successive frames which may or may not contain the comma character.

Detail Description Paragraph - DETX (36):

[0076] FIG. 8 shows the internal structure of an exemplary TBS. The TBS has two separate data paths: one from the line (left) side to the system (right) side (upper portion of FIG. 8), and one from the system side to the line side (lower portion of FIG. 8). The line-to-system side begins with parallel Telecombus interface 10 and PRBS generators and monitors (for testing), which then presents the dataflow to three copies (respectively labelled "A", "B" and "C" in FIG. 8) of the following blocks (supporting the working, protection, and auxiliary flows): memory switching stage 12, disparity encoder 14, serializer 16, and transmit circuits 18. The system-to-line side begins with **LVDS** receivers 20, which pass data to data recovery units 22 (as in the TSE), then to 8b/10b decoders 24, then to PRBS units 26, then to memory switching stages 28, which feed parallel Telecombus interface 30. The system-to-line side is triplicated (and again labelled "A", "B" and "C") for the working, protection, and auxiliary paths, up to the parallel Telecombus interface. Microprocessor interface 32 is separate, but has bus-based access to registers throughout the

US-PAT-NO: 6671271

DOCUMENT-IDENTIFIER: US 6671271 B1

TITLE: Sonet synchronous payload envelope pointer control system

DATE-ISSUED: December 30, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Takemura; Takenao	Plano	TX	N/A	N/A
Doan; Tri H.	Plano	TX	N/A	N/A
Okutsu; Akihiko	Plano	TX	N/A	N/A
Pudu; Srinivas	Richardson	TX	N/A	N/A

US-CL-CURRENT: 370/352, 370/465 , 370/907

ABSTRACT:

A multiported integrated circuit performs pointer processing at the SONET STS and VT levels, and removes overhead information from a received electrical signal derived from an optical SONET signal. The integrated circuit operates to extract STM traffic and ATM traffic from the received SONET signal, in response to provisioning information received from a management and control unit. The extracted STM traffic is then combined with path switching information, and forwarded out a pair of interfaces, which enables path selection within an STM switch fabric within a local line unit and within a switch fabric on a partner line unit in an active/standby pair of line units. The path switching information is also output from the integrated circuit for transmission to a pair of ATM switch fabric units.

17 Claims, 17 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 17

---------- KWIC ---------

Abstract Text - ABTX (1):
A multiported integrated circuit performs pointer processing at the SONET STS and VT levels, and removes overhead information from a received electrical signal derived from an optical SONET signal. The integrated circuit operates to extract STM traffic and ATM traffic from the received SONET signal, in response to provisioning information received from a management and control unit. The extracted STM traffic is then combined with path switching information, and forwarded out a pair of interfaces, which enables path selection within an STM switch fabric within a local line unit and within a switch fabric on a partner line unit in an active/standby pair of line units. The path switching information is also output from the integrated circuit for transmission to a pair of ATM switch fabric units.

TITLE - TI (1):

Sonet synchronous payload envelope pointer control system

Brief Summary Text - BSTX (2):
The invention relates generally to communication systems, and more specifically to a multiported integrated circuit for interfacing a local STM switch fabric and an ATM switch fabric unit to a **SONET** ring.

Brief Summary Text - BSTX (3):
As it is generally known, **SONET** (Synchronous Optical Network) defines a set of standards for a synchronous optical hierarchy that has the flexibility to transport many digital signals having different capacities. A corresponding international synchronous digital hierarchy (**SDH**) standard provides a set of definitions analogous to those of **SONET**. The synchronous nature of **SONET** is provided by a receive side and a transmit side clock in each network element (NE). In order to synchronize the receive and transmit clocks, a **SONET** network element, such as an add-drop multiplexer, includes circuitry to recover clock signals from various sources that may be available, and to distribute highly accurate clocks internally based on such recovery.

Brief Summary Text - BSTX (4):
A central timing source provides a Building Integrated Time Source, also referred to as a "BITS" clock, that may be provided out-of-band to each network element in a **SONET** ring. If a network element is for some reason not able to receive the BITS clock directly, an embedded clock may be recovered by that device from an incoming line that should reflect the centrally provided BITS clock.

Brief Summary Text - BSTX (5):
The basic building block in **SONET** is a synchronous transport signal level-1 (STS-1), which is transported as a 51.840-Mb/s serial transmission using an optical carrier level-1 (OC-1) optical signal. Higher data rates are transported using **SONET** by multiplexing N lower level signals together. To this end, **SONET** defines optical and electrical signals designated as OC-N (Optical Carrier level-N) and STS-N (Synchronous transport signal level-N), where OC-N and STS-N have the same data rate for a given value of N. Accordingly, just as STS-1 and OC-1 share a common data rate of 51.84 Mb/s, OC-3/STS-3 both have a data rate of 155.52 Mb/s.

Brief Summary Text - BSTX (6):
Information transported via an STS-1 signal is organized as frames, each having 6480 bits (810 bytes). An STS-1 frame includes transport overhead and a Synchronous Payload Envelope (SPE). The SPE includes a payload, which is typically mapped into the SPE by what is referred to as path terminating equipment at what is known as the path layer of the **SONET** architecture. Line terminating equipment, such as an OC-N to OC-M multiplexer, is used to place an SPE into a frame, along with certain line overhead (LOH) bytes. The LOH bytes provide information for line protection and maintenance purposes. The section layer in **SONET** transports the STS-N frame over a physical medium, such as optical fiber, and is associated with a number of section overhead (SOH) bytes. The SOH bytes are used for framing, section monitoring, and section level equipment communication. Finally, a physical layer in **SONET** transports the bits serially as either electrical or optical entities.

Brief Summary Text - BSTX (8):
The pointer value enables a **SONET** network element to operate in the face of certain conditions which may, for example, cause the STS-1 frame rate to become faster or slower than the SPE insertion rate. This situation may arise when the clock of the NE must be derived from a relatively less accurate clock source, in order to continue operation, when a more accurate source, such as

serial links 66.

Detailed Description Text - DETX (23):
FIG. 5 shows an ATM configuration of the disclosed network element, including the two LUs 60a and 60b, the ATMUs 70a and 70b, the MCU 62 and ATM service units 80a through 80f. The ATM Interworking service unit 80a includes a service interface to a 10/100BaseT LAN, the native ATM service unit 80b includes a service interface to an OC-3 based cell relay connection, and a pair of ATM Interworking Service Units 80c and 80d include service interfaces to a DS-1 frame relay connection. The service units in FIG. 5 are connected via an active/standby pair of ATMUs 70a and 70b to a pair of OC-12 LUs 60a and 60b. The service units 80c and 80d are configured as an active/standby pair. The ATM subtending ring service units 80e and 80f provide a service side interface to a **SONET** ring carrying ATM cells.

Detailed Description Text - DETX (24):
During operation of the embodiment shown in FIG. 5, ATM cells carried over STS signals within the **SONET** ring 61 are routed by the line units 60a-60b over STS-12 datapath connections 81 to each of the ATM switch fabrics within the ATM switch fabric units 70a and 70b. The ATM switch fabric units 70a and 70b in turn direct the ATM cells, based on VPI/VCI values within the cell headers, to the appropriate destination service units as indicated by ATM virtual connections established through the ATM switch fabric.

Detailed Description Text - DETX (26):
FIG. 7 is a functional block diagram of an illustrative line unit 100. The line unit 100 provides an optical interface to a **SONET** ring at the line side of the disclosed network element. The line unit 100 is shown including a signal routing ASIC 102, which is coupled to an optical receiver 104, an optical transmitter 106, ATMU Low Voltage Differential Signaling (**LVDS**) receivers 108, ATMU transmitters 110, and an STM switch fabric ASIC 114. ATMU transmitters 110 and ATMU receivers 108 are, for example, shown using **LVDS** devices. The STM switch fabric ASIC 114 is shown including service unit transmit interfaces 116 and service unit receive interfaces 118.

Detailed Description Text - DETX (27):
During operation of the line unit 100, the optical receiver 104 receives for example a **SONET** formatted OC-12 or OC-3 optical signal, carrying an STS-12 or STS-3 signal respectively, or any suitably formatted signal. The optical receiver 104 passes electrical clock signals 124 and data signals 126 that reflect the received **SONET** signal to the signal routing ASIC 102. The signal routing ASIC 102 extracts STS frames from the STS signal, performs pointer interpretation to locate the beginnings of payloads and virtual tributaries within the received frames, and also extracts line, section and path overhead data. The extracted overhead data 128 is sent by the signal routing ASIC 102 to a management and control unit (MCU) for further processing.

Detailed Description Text - DETX (33):
The line unit 100 further includes various clock related elements including an extended synchronization module (ESM) 120, which, in combination, provide STM synchronization clocks to the line unit and other units within the device. Specifically, a timing reference switch 145 is controlled by the output of synchronization switch controller logic 146. A number of inputs 147 to the synchronization switch controller logic 146 provide indication of whether the ESM 120 is present, whether the active/standby partner line unit is present, and whether the **SONET** signal on the line side is present on either the local or partner line unit.

Detailed Description Text - DETX (34):

US-PAT-NO: 6539051

DOCUMENT-IDENTIFIER: US 6539051 B1

TITLE: Parallel framer and transport protocol with distributed framing and continuous data

DATE-ISSUED: March 25, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Grivna; Edward L.	Brooklyn Park	MN	N/A	N/A

US-CL-CURRENT: 375/219, **370/470** , **370/474** , **370/476** , 375/222 , 375/225 , 375/257 , 375/265 , 375/295 , 375/316

ABSTRACT:

A method and system for serially communicating a stream of data characters having bit-interleaved framing information. One embodiment discloses a method for interleaving a single bit of a frame marker sequence to each data character to demarcate each of the data characters and then serializing the data. The transmitting device serially transmits the data characters with bit-interleaved framing at a high transmission bit rate, over a single communication link. The receiving device captures the data stream and de-serializes the data. It then locates the bit position of the character boundary by detecting a predetermined frame marker sequence located in the same bit position over consecutive data characters. The offset is used to frame the data. A character rate greater than 70 MHz can be realized and a bit transmission rate of greater than 1 Gbit/second can be achieved.

25 Claims, 11 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 12

---------- KWIC ---------

Brief Summary Text - BSTX (5):

The telephone companies, however, abandoned this method of framing when high-speed transmission, e.g., in excess of 45 Mbits/second, was required. At data rates faster than T3, voice and data are transmitted with **SONET** protocols which use character-based framing. **SONET** protocols are used for data rates greater than 51 Mbits/second. In **SONET** protocols, a sequence of framing characters is used to mark the frame boundaries. At the receiving end, detection of the sequence of framing characters provides the frame boundary.

Brief Summary Text - BSTX (10):

FIG. 1B illustrates an improved communication system 190. To improve the method, the parallel bus of FIG. 1A was replaced with a set of **LVDS** (Low Voltage Differential Signaling) based serial links. Standard **LVDS** devices can accept and communicate parallel buses of 24-bits in width including a clock across four differential signal paths. The data is sent on several separate serial data streams, each carrying a subset of the total number of bits, along with a separate signal for the clock. According to this improved method, data is only serialized and not scrambled or encoded.

Brief Summary Text - BSTX (12):

A disadvantage associated with the previous methods is that the multiple signals that make each communication channel (parallel or multiple **LVDS** serial) have to be delay matched, i.e., they have to be measured to the same electrical length. This is due to the fact that at the receiving end, data recovery is relative to the clock time reference received on one of the **LVDS** signals. If any signal path is slightly longer than the other, the receiving end samples the bits at the wrong place. Therefore, a slight difference in length between these four differential pairs may disturb the integrity of the data information captured at the receiving end.

Drawing Description Text - DRTX (4):

FIG. 1B depicts an improved method of the transmission described in FIG. 1A, using multiple **LVDS** serial links in parallel, reducing the backplane signal density.

Current US Cross Reference Classification - CCXR (1):

370/470

Current US Cross Reference Classification - CCXR (2):

370/474

Current US Cross Reference Classification - CCXR (3):

370/476

US-PAT-NO: 6157638

DOCUMENT-IDENTIFIER: US 6157638 A

TITLE: High density packet switch with high speed interfaces and method for using same

DATE-ISSUED: December 5, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tayloe; Daniel Richard	Phoenix	AZ	N/A	N/A
Armbruster; Peter Joseph	Chandler	AZ	N/A	N/A
Rao; Kajana Aswath	Chandler	AZ	N/A	N/A

US-CL-CURRENT: 370/358, 340/2.27 , 370/389 , 370/463

ABSTRACT:

A high speed packet switch (100) is provided which uses a fabric size of 128.times.128 and operates at a 2.5 Gbps rate. Parallel data transport techniques are used to obtain the 2.5 Gbps data rate while operating internal switches (160) at slower rates. The packet switch fabric is fabricated on a single ASIC using high speed CMOS.

11 Claims, 2 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 2

---------- KWIC ---------

Brief Summary Text - BSTX (7):

In addition, the currently available single stage switches are primarily configured with eight inputs and eight outputs. Some currently available single stage switches are configured with eight inputs and eight outputs. Typically, the data rates for the inputs are usually at either the 155 Mbps OC-3 rates or the 622 Mbps OC-12c rates, where OC indicates an optical signal. The Synchronous Optical Network (SONET) hierarchy is based on a fundamental unit which is equal to 51.84 Mbps. For example, an OC-1 nomenclature implies a 51.84 Mbps rate, and an OC-3 input implies a 1.5 Mbps rate (3*51.84 Mbps).

Detailed Description Text - DETX (9):

In a preferred embodiment, high density packet switch 100 comprises a number of Low Voltage Differential Signaling (LVDS) input lines 110, a number of LVDS output lines 120, and a switching network 105 coupled between LVDS input lines 110 and LVDS output lines 120.

Detailed Description Text - DETX (15):

In a preferred embodiment, input modems 130 are LVDS devices, although this is not required for the invention. LVDS is a serial interface methodology that operates at rates above 1.0 Gbps for distances of over ten meters. The signals are differential, and these signals require two 50 Ohm controlled impedance transmission lines per bit. Alternate embodiments can be constructed using

different devices.

Detailed Description Text - DETX (16):
In a preferred embodiment, 512 **LVDS** input modems 130 are used, although this is not required for the invention. In alternate embodiments, the number of modems does not have to be equal to 512.

Detailed Description Text - DETX (22):
In a preferred embodiment, output rate change device 180 is coupled to the input side of each of the output modems 190. In this case, output modems 190 are **LVDS** devices. Alternate embodiments can be constructed using different device types.

Detailed Description Text - DETX (39):
In a preferred embodiment, the switch is used to interface OC-48 input data streams where OC indicates an optical signal (carrier). The Synchronous Optical Network (**SONET**) hierarchy is based on a fundamental unit which is equal to 51.84 Mbps. For example, an OC-1 nomenclature implies a 51.84 Mbps rate, and an OC-48 input implies a 2.5 Gbps rate (48*51.84 Mbps).

Claims Text - CLTX (2):
a plurality of input modems coupled to a number of Low Voltage Differential Signaling (**LVDS**) input lines, said number of **LVDS** input lines comprising at least sixty-four input groups, each input group having at least four input bits, each input bit comprising two **LVDS** input lines;

Claims Text - CLTX (8):
a plurality of output modems coupled to said output rate change devices, said output modems being coupled to a number of **LVDS** output lines, said number of **LVDS** output lines comprising at least sixty-four output groups, each output group having at least four output bits, each output bit comprising two **LVDS** output lines.

Claims Text - CLTX (15):
8. The packet switch as claimed in claim 1, wherein said input modems comprise **LVDS** devices.

Claims Text - CLTX (16):
9. The packet switch as claimed in claim 1, wherein said output modems comprise **LVDS** devices.

Current US Original Classification - CCOR (1):
370/358

Current US Cross Reference Classification - CCXR (2):
370/389

Current US Cross Reference Classification - CCXR (3):
370/463

Other Reference Publication - OREF (1):
IEEE Standard for Low-Voltage Differential Signals (**LVDS**) for Scalable Coherent Interface (SCI), IEEE, New York, 1996, All pages.

US-PAT-NO: 6498792

DOCUMENT-IDENTIFIER: US 6498792 B1
See image for Certificate of Correction

TITLE: Method and apparatus for switching signals of multiple different communication protocols

DATE-ISSUED: December 24, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Johnson; Gary P.	McKinney	TX	N/A	N/A
Moubarak; Roland J.	Garland	TX	N/A	N/A
Shimbashi; Masahiro	Kawasaki	N/A	N/A	JP
Shirota; Katsuya	Richardson	TX	N/A	N/A
Chen; David X.	Plano	TX	N/A	N/A

US-CL-CURRENT: 370/388, 370/376 , 370/466

ABSTRACT:

A telecommunications switching apparatus (10) includes optical paths (16-19) coupled to interface cards (26-29), which in turn are coupled to a switching circuit (41-42). The switching circuit is coupled to a plurality of universal connectors (71-74), each of which is coupled to an auxiliary connector (77-78). The universal connectors can each removably receive any one of several types of switching circuit cards (101-104), which each utilize a respective one of several different communication protocols. An auxiliary circuit card (107-108) may be provided in the associated auxiliary connector, in order to support switching circuit cards that use certain communication protocols. The optically transmitted information includes segments formatted according to respective communication protocols, and is converted from optical to electrical form by the interface cards. The switching circuit then routes each segment to a respective universal connector containing a switching circuit card that effects switching according to the communication protocol of that segment.

18 Claims, 1 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 1

---------- KWIC ---------

Brief Summary Text - BSTX (6):

One existing system uses a line card to terminate a fiber optic path which carries information formatted according to the SONET (Synchronous Optical NETwork) industry standard. According to the SONET standard, information is transmitted in packets known as frames, where each frame includes some overhead information and several data segments. Each data segment includes data formatted according to one of several different industry standard communication protocols, and different data segments in the same frame may conform to different communication protocols. In this existing system, the line card is coupled by respective different interfaces to respective dedicated connectors,

where each connector corresponds to a respective communication protocol and can each be detachably coupled to a switching circuit card that effects switching according to that respective protocol. The line card terminates the optical path by converting the transmitted information from an optical format to an electrical format. Further, the line card terminates the SONET communication by demapping the SONET frame, so as to organize the data segments according to the specific communication protocols by which the data is formatted. The line card then routes each data segment to the connector and switching circuit card that correspond to the same communication protocol as that data segment. While this existing approach has been generally adequate for its intended purposes, it has not been satisfactory in all respects.

Brief Summary Text - BSTX (7):

More specifically, because each connector must be dedicated to a particular communication protocol, extra connectors must be provided for each communication protocol of interest, which leads to a relatively large number of extra connectors of various types in any given system, which in turn increases the overall system size. The larger the system, the more space it takes up in a central facility, a terminal application, or the like. Further, providing separate and different types of electrical interfaces to the respective types of connectors for the various communication protocols has the effect of increasing the complexity and cost of the backplane wiring in the system. Moreover, maintenance of the system is complicated by the fact that maintenance personnel must be careful to plug a given switching circuit card only into the proper connector, not just to ensure proper system operation, but also to avoid possible damage to system circuitry. In addition, due to the fact that each line card not only terminates a fiber optic path, but also has to terminate the SONET frame and then route the data segments to respective different switching circuits, the circuitry of the line cards is relatively sophisticated and expensive.

Detailed Description Text - DETX (3):

In the disclosed embodiment, the communication paths 16-19 are each implemented as a fiber optic path, and information is transmitted along these fiber optic paths using an industry standard known as SONET (Synchronous Optical NETwork). According to the SONET standard, information is transmitted in packets which are known as frames, where each frame includes some overhead information and several data segments. Each data segment includes data formatted according to one of several different industry standard communication protocols. In the disclosed embodiment, these protocols include the asynchronous transport mode (ATM), virtual tributary (VT), and Internet protocol (IP). However, the present invention is compatible with other existing or future communication protocols. Further, although the communication paths 16-19 in the disclosed embodiment are fiber optic paths which use the SONET standard, it will be recognized that other standards or types of communication paths could be used.

Detailed Description Text - DETX (8):

The switching apparatus 10 also has four universal connectors 71-74, and two ATM Processing Control (APC) connectors 77 and 78. The universal connectors 71 and 72 and the APC connector 77 are the working components, whereas connectors 73-74 and 78 are the corresponding protection components. The universal connectors 71-74 are each coupled with the switching circuit 41 through a respective interface 81-84, and with the switching circuit 42 through a respective interface 86-89. The APC connector 77 is coupled by an interface 91 to each of the universal connectors 71 and 72. Similarly, the APC connector 78 is coupled by an interface 93 to each of the universal connectors 73 and 74. The control circuit 36 is coupled by lines 97 to the universal connectors 71-74 and the APC connectors 77 and 78. In the disclosed embodiment, the interfaces 81-84 and 86-89 which couple the connectors 71-74 to the switching circuits 41 and 42 are effectively identical to the interfaces 46-49, 51-54 and 56-59 which couple the cards 31-34 to the switching circuits 41 and 42. In the disclosed embodiment, all of these interfaces are implemented using a type of interface

known to those skilled in the art, and use a technique known in the art as low voltage differential signaling (**LVDS**).

Detailed Description Text - DETX (13):
As discussed above, the switching circuit 42, universal connectors 73-74, APC connector 78, switching circuit cards 103 and 104, and APC circuit cards 108 respectively provide back-up protection for the switching circuit 41, universal connectors 71-72, APC connector 77, switching circuit cards 101-102 and APC circuit card 107. The protection portion of the system will be set up to essentially mirror the working portion of the system. Thus, the universal connector 73 will include a switching circuit card 103 which is of the type that effects switching according to the ATM communication protocol, the universal connector 74 will include a switching circuit card 104 which is of the type that effects switching according to the VT communication protocol, and the APC connector 78 will be coupled to an APC circuit card 108. For simplicity, the following explanation discusses the operation of the system primarily with reference to the working components, and with only limited reference to the protection components. Also, the following discussion focuses on communication path 16 and line card 26, but it will be recognized that the discussion is equally applicable to the other communication paths 17-19 and the other cards 27-29. As discussed above, information received across communication path 16 will be in the form of optical communications which conform to the **SONET** standard, involving a series of frames that each include a plurality of data segments. Each data segment will include information to be handled according to one of the ATM protocol or the VT protocol. The segments in a given frame may all be formatted for the ATM protocol, may all be formatted for the VT protocol, or may be a mixture of ATM and VT information.

Detailed Description Text - DETX (14):
The line card 26 terminates the optical communication, in that it converts the optical signal into electrical signals, which are supplied across the interface 46 to the switching circuit 41. The line card 26 does not terminate the **SONET** payload, or in other words does not break up each **SONET** frame and then organize the information in that frame by communication protocol. Instead, the line card 26 passes received **SONET** frames across the interface 46 to the switching circuit 41, in an electrical rather than optical format.

Detailed Description Text - DETX (15):
The switching circuit 41 terminates the **SONET** frames, in particular by extracting the various data segments and organizing them according to whether they are formatted for the ATM protocol or the VT protocol. The data segments which represent ATM traffic are then sent through the interface 81 and connector 71 to the switching circuit card 101, whereas the data segments which represent VT traffic are sent through the interface 82 and connector 72 to the switching circuit card 102. The switching circuit card 101 effects switching according to the ATM protocol, with support from the APC circuit card 107, and the switching circuit card 102 effects switching according to the VT protocol.

Detailed Description Text - DETX (16):
Outbound ATM traffic from the switching circuit card 101 is sent through the connector 71 and interface 81 to the switching circuit 41, and outbound VT traffic from the switching circuit card 102 is sent through the connector 72 and interface 82 to the switching circuit 41. The switching circuit 41 then reformats this outbound ATM and VT traffic into **SONET** frames. The resulting **SONET** frames are then transmitted across the interface 51 to the line card 26. Unless a fault has been detected in the switching circuit 41, the multiplexer 31 in line card 26 will be set to receive information across interface 51 from the circuit 41, rather than across interface 56 from the circuit 42. The line card 26 takes the **SONET** frames received across interface 51, converts them from electrical format into optical format, and then transmits them across the communication paths 16 of the communication path section 22.

Detailed Description Text - DETX (18):
A further advantage is that the provision of universal slots simplifies maintenance considerations, because a given switching circuit card can be plugged into any connector, whereas conventional dedicated connectors make it necessary to ensure that a given card is plugged only into the proper type of connector, in order to avoid both system inoperability and possible damage to circuitry. Yet another advantage is that, by avoiding separate dedicated paths to various types of dedicated connectors, the complexity and cost of the backplane wiring is reduced. Yet another advantage is that, because the line cards and the tributary cards of the disclosed embodiment terminate only the fiber optic transmission, rather than the **SONET** frames, these cards have reduced complexity in comparison to existing line cards, which in turn translates into reduced cost. Still another advantage is that the cross-coupled interfaces between the switching circuits and the universal connectors facilitate bank switching in the event of card failures.

Detailed Description Text - DETX (20):
A further example is that the disclosed embodiment uses communication paths which are fiber optic paths and which utilize the **SONET** standard, but it will be recognized that the present invention could encompass the use of a non-optical and/or a non-**SONET** approach. It will also be recognized that direct connections disclosed herein could be altered, such that two disclosed components or elements would be coupled to one another through an intermediate device or devices, without being directly connected, but while still realizing the present invention. Other substitutions and alterations are also possible without departing from the spirit and scope of the present invention, as defined by the following claims.

Claims Text - CLTX (11):
11. An apparatus according to claim 10, wherein said communication information is transmitted optically through said communication paths in the form of **SONET** frames, said **SONET** frames each including a plurality of said information segments, said interface circuits effecting said conversion of said **SONET** frames from optical to electrical format and then forwarding said **SONET** frames to said switching section, and said switching section extracting said information segments from said **SONET** frames received from said interface circuits.

Claims Text - CLTX (18):
18. A method apparatus according to claim 12, wherein said transmitting step includes the step of optically transmitting information through said communication paths in the form of **SONET** frames each containing a plurality of said information segments, converting said **SONET** frames from an optical to an electrical format in an interface circuit and then forwarding said **SONET** frames to said switching section, and then extracting said information segments from said **SONET** frames in said switching section.

Current US Original Classification - CCOR (1):
370/388

Current US Cross Reference Classification - CCXR (1):
370/376

Current US Cross Reference Classification - CCXR (2):
370/466

Other Reference Publication - OREF (9):

Tai H. Noh, "ATM Scenarios for **SDH/SONET** Networks XP-000750438," Bell Labs Technical Journal, Jan., 1998, 13 pages.

Other Reference Publication - OREF (13):
Cerent 454.TM. High Speed **SONET/SDH** Transport System, ALTS trade show, Las Vegas, Nevada on or about Dec., 1998.

Other Reference Publication - OREF (25):
"S/DMS TransportNode `OC-3 Express`--Cost-Effective **SONET** Transport for Low-Capacity Applications", Northern Telecom Marketing Publications, Issue 1, pp. 1-31, Sep. 27, 1996.

US-PAT-NO: 6301269

DOCUMENT-IDENTIFIER: US 6301269 B1

TITLE: ATM switching system and method with propagation delay compensation

DATE-ISSUED: October 9, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tayloe; Daniel Richard	Phoenix	AZ	N/A	N/A
Armbruster; Peter Joseph	Chandler	AZ	N/A	N/A
Rao; Kajana Aswath	Chandler	AZ	N/A	N/A

US-CL-CURRENT: 370/519, 370/399 , 375/362

ABSTRACT:

A switch system (20) switches at least sixty-four asynchronous transfer mode (ATM) input data streams (22) into at least sixty-four ATM output data streams (24). The switch system (20) includes a backplane assembly (38) having integral data transmission lines, integral clock transmission lines, and discrete slots (36). A single stage space switch circuit card (26), a clock circuit card (28), and input circuit cards (30) are connected to separate slots (36) in the backplane assembly (38). The integral data transmission lines are coupled between the input circuit cards (30) and the switch circuit card (26) and the integral clock transmission lines are coupled between the clock circuit card (28) and the input circuit cards (30). Data path lengths for the integral data transmission lines differ in the backplane assembly (38), and clock path lengths for the clock transmission lines differ in the backplane assembly. A timing compensation element (86) on each of the input circuit cards (30) imparts a time delay to one of the ATM input data streams (22) to compensate for data and clock path length differences so the each of the ATM input data streams (22) arrive at the single stage switch (26) substantially synchronously.

21 Claims, 6 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

---------- KWIC ---------

Detailed Description Text - DETX (11):

Each of ATM input data streams 22 has a synchronous optical network (SONET) data rate of at least 155 megabits per second and a data rate of approximately 2.5 gigabits per second in the preferred embodiment. Likewise, each of ATM output data streams 24 has this same rate. Furthermore, switch system 20 is a non-blocking switch system configured to input 128 ATM input data streams 22 and output 128 ATM output data streams 24.

Detailed Description Text - DETX (13):

In order to accomplish this high data throughput, the interface between space switch 26 and I/O circuit cards 30 is preferably implemented using low

voltage differential signaling (LVDS) semiconductor components, although other technologies are also suitable. LVDS technology is a low swing, differential signaling technology which allows single channel data transmission at hundreds of megabits per second (Mbps). Its low swing and current mode driver outputs create low noise and low power consumption at high frequencies. In addition, the differential data transmission method used in LVDS technology is less susceptible to common-mode noise than single-ended schemes. However, LVDS signals are differential signals. That is, each signal is conveyed using two transmission lines. The use of two transmission lines to convey each signal exacerbates the problem of routing numerous input and output data transmission lines 40 and 42 (FIG. 1) between I/O circuit cards 30 (FIG. 1) and switch card 26 (FIG. 1).

Detailed Description Text - DETX (38):

Input interface circuit 82 includes interface circuit 116 configured to receive ATM data cell 114. Interface circuit 116 is preferably a SONET interface circuit, althogh other technology may be suitable. At interface circuit 116, ATM data cell 114 passes through framing (e.g., SONET Framing) and ATM Cell Processing blocks in which the pre-existing ATM header information is anaylzed. Per convention, invalid ATM data cells may be discarded, and an error indication is preferably sent to controller 34.

Detailed Description Text - DETX (43):

In connection with the path establishment activities, for data type cells, a cell priority determiner element 122 coupled between SONET interface circuit 116 and buffer 84 further defines the assigned switching priority for ATM data cell 114. In addition, cell priority determiner 122 includes a cell drop logic circuit 124. Cell drop logic circuit 124 checks the cell loss priority bit in the header field of ATM data cell 114 to determine if the data cell 114 is to be dropped. In an alternative embodiment, cell drop logic circuit 124 checks the cell loss priority bit to determine if the switching priority for ATM data cell 114 is to be decreased. A virtual circuit (VC) table 126 is used by cell drop logic circuit 124 to indicate which virtual circuit ATM data cell 114 is associated with.

Detailed Description Text - DETX (71):

In summary, a switch system and method are provided for switching a plurality of input data streams into a plurality of output data streams. The system includes a non-blocking, single stage space switch capable of switching a large number of high speed input data streams. The switch is implemented in low voltage differential signaling (LVDS) semiconductor components in order to accommodate the high data rates of the input data streams. The system size is greatly reduced and system reliability is increased at low cost by replacing the few uniform length cable assemblies of prior art systems with a backplane assembly having a multiplicity of transmission lines on a printed circuit board medium. In addition, a timing compensation element is incorporated into the system to mitigate propagation delays associated with differing path lengths of the differing transmission lines.

Claims Text - CLTX (38):

12. A system as claimed in claim 11 wherein said first and second input data streams are included in said plurality of input data streams, each of said plurality of input data streams having a synchronous optical network (SONET) data rate of at least 2.5 gigabits per second, and said single stage space switch is configured to switch at least sixty-four of said input data streams into at least sixty-four of said output data streams substantially synchronously.

Claims Text - CLTX (39):

13. A system as claimed in claim 11 wherein said single stage space switch

is implemented using low voltage differential signaling (LVDS) semiconductor components.

Current US Original Classification - CCOR (1):
370/519

Current US Cross Reference Classification - CCXR (1):
370/399

US-PAT-NO: 6208666

DOCUMENT-IDENTIFIER: US 6208666 B1
See image for Certificate of Correction

TITLE: System and method for maintaining timing synchronization in a digital video network

DATE-ISSUED: March 27, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lawrence; Peter H.	Smyrna	GA	N/A	N/A
Dunn; Bryan W.	Newnan	GA	N/A	N/A
Eshleman; Matthew A.	Lilburn	GA	N/A	N/A

US-CL-CURRENT: 370/503, 370/498

ABSTRACT:

A novel system and method for maintaining timing synchronization in a digital video network, in conjunction with a digital video and data delivery system, makes possible the delivery of digital video content, bi-directional data services, such as Internet data, and plain old telephone service (POTS) to an end user over a communications channel. The channel is typically the copper wire pair that extends between a telephone company central office and a residential premises, but may be any communication medium that supports the communication of compressed digital video, bi-directional data, such as Internet data, and POTS, and indeed, may be a wireless connection. The digital video and data delivery system capitalizes on a bus, or broadcast backplane, created by circuitry contained within the central office. The broadcast backplane enables a plurality of video program data to be available to each end user, and allows a plurality of end users access to a plurality of video programming content without the necessity of delivering the entire program content to each end user.

15 Claims, 48 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 48

---------- KWIC ---------

Detailed Description Text - DETX (5):

FIG. 1A is a high level system view illustrating the overall topology in which the system and method for maintaining timing synchronization in a digital video network of the present invention resides. Included in system topology 10 are telephone company programming and control center (TPCC) 100, central office 400, and customer premises 1300. TPCC 100 receives input from local broadcaster 12, which provides broadcast television signals, content provider 11, which provides digital video signals in the form of MPEG-2 encoded video, and data from Internet service provider (ISP) 14. While illustrated herein as transporting Internet data, indeed any data, such as for example but not limited to local area network (LAN) or any digital data may be transported in accordance with the present invention. TPCC 100 communicates with central office 400 over **SONET** network (synchronous optical network) 150. While a

single central office is shown for simplicity, TPCC 100 may communicate with a plurality of central office locations 400 over SONET network 150. SONET network 150 represents one manner in which a TPCC may communicate with central office locations and is typically the internal telephone company network that connects multiple central offices with each TPCC. SONET network 150 is used for illustrative purposes only. Other internal networks, such as, for example but not limited to, an SDH (synchronous digital hierarchy) network or any method of communicating between TPCC 100 and central office locations 400 may be used to communicate between TPCC 100 and central office 400. Central office 400 communicates with customer premises 1300 over communication channel 16. Communication channel 16 can be any communication channel capable of supporting the communication of compressed digital video, bi-directional Internet data and POTS, and is illustratively carried over the copper wire pair over which conventional telephone signals are communicated. Other communication channels, for example but not limited to a wireless communication channel such as an LMDS (local multipoint distribution system), may be used to communicate between central office 400 and customer premises 1300. Located at customer premises 1300 are intelligent network interface (INI) 1350 to which are connected computer system 1355, telephone 1360, fax machine (not shown), and television 1365. It is also possible to provide an additional digital telephony communication line to which may be connected a fax machine. The digital video and data delivery system and method of the present invention operate to allow TPCC 100 to deliver to central office 400, and central office 400 to deliver to customer premises 1300 over a communication channel 16, compressed digital programming, bi-directional Internet data, and POTS.

Detailed Description Text - DETX (7):

FIG. 2 is a schematic view illustrating the delivery of video content from content provider 11 to TPCC 100. Content provider 11 receives an analog video signal illustratively via satellite 17. Alternatively, content provider 11 receives digitally encoded video signals illustratively via satellite 17. It should be understood that audio content accompanies the video signals referred to herein, and when referring to video, or compressed digital video, it is understood that the audio signal is included. Content provider 11 delivers the analog (or digital) video signals over network 13 to a plurality of TPCCs 100. Network 13 can be, for example but not limited to, a satellite delivery network or possibly a SONET network similar to SONET network 150 of FIG. 1. TPCCs 100 receive local broadcast video programming from local broadcasters 12.

Detailed Description Text - DETX (8):

FIG. 3 is a schematic view illustrating the architecture that connects TPCC 100 to central offices 400. As discussed above, TPCC 100 receives video, in the form of an analog or a digital signal from content provider 11, local broadcast television from local broadcaster 12, and Internet data from ISP 14. TPCC 100 integrates the aforementioned content and provides it to central offices 400 over Telco SONET network 150, or via any network used to communicate between TPCC 100 and central office locations 400.

Detailed Description Text - DETX (9):

FIG. 4 is a block diagram illustrating the components of the present invention that reside within TPCC 100. Within TPCC 100 bi-directional data from ISP 14, video content from content provider 11 (of FIGS. 1 and 2) and local programming from local broadcaster 12 are combined. Bi-directional Internet data are supplied from ISP 14 over connection 128 to router 101. Router 101 communicates over connection 112 with ATM switch 102, which communicates with SONET add-drop multiplexer 106 over connection 114. SONET add-drop mux 106 is shown for illustrative purposes only, and would be an SDH multiplexer if an SDH network were implemented in place of SONET network 150. In this manner, Internet data are processed by TPC 100 and forwarded to central offices 400 over SONET network 150. Also communicated over connection 114 are management and control data from system management workstation 325, which will be described in detail below. Video content is supplied from content provider

11 over connection 126 to satellite receiver 104. If the video content supplied from content provider 11 is in the form of an analog signal, then it is supplied over connection 115 to MPEG-2 encoder 109 for conversion to MPEG-2 format. Although MPEG-2 is used in the preferred embodiment, any digital compression technique may be used to generate the compressed digital video signal. If the video content supplied by content provider 11 is in the form of a digital signal, then it is supplied directly to video control shelf 200 via connection 118. Connection 118 is illustratively a plurality of DS-3 connections and in the preferred embodiment is a total of seven (7) DS-3 connections. A DS-3 connection provides approximately 45 megabits/second (Mb/s) of data transfer, and is used herein illustratively.

Detailed Description Text - DETX (11):

Also connected to video control shelf 200 over connection 117 is system management workstation (SMW) 325. SMW 325 provides supervisory, management and control functions for TPCC 100 and will be discussed in detail with reference to FIG. 8. SMW 325 also connects to ATM switch 102 over connection 116, whereby management and control information is sent through ATM switch 102 and over connection 14 to **SONET** add/drop mux 106 for placement on **SONET** network 150. In this manner, management and control information is delivered to and received from central office 400.

Detailed Description Text - DETX (12):

Video control shelf 200 inserts local program guide and control information into the digital video program by replacing a null MPEG-2 packet that is not used to transport video data. This local program guide information comes from SMW 325, the workstation responsible for monitoring and controlling the digital video and data delivery system. The program guide database is received from a centralized provider or may be locally generated. Video control shelf 200 can also be used to insert software update data for customer premise information by replacing a null MPEG-2 packet that is not used to transport video data. The video programming with the newly inserted data then enters the telephone company (telco) private **SONET** network 150 via **SONET** add-drop mux 106. Router 101 isolates the internal telco data delivery network from the Internet, routing only the appropriate packets to ISP 14. ATM switch 102 provides a robust interconnection to the switches in the individual central offices 400 providing Internet data to the system. Furthermore, router 101 and ATM switch 102 exchange Internet data in both upstream (from customer premises toward central office to TPCC) and downstream (from TPCC to central office, to customer premises) directions.

Detailed Description Text - DETX (15):

The output of each video control module pair 250 is provided via DS-3connection 119 to **SONET** add-drop multiplexer 106. Also included in video control shelf 200 is shelf processor module pair 300. The operation of video control module 250 will be discussed in detail with reference to FIG. 6 and the operation of shelf processor module 300 will be discussed in detail with reference to FIG. 7. The digital video and data delivery system of the present invention currently supports up to eight digital video program groups, however, it is foreseeable that in the future additional program groups may be supported. A program group is defined as a single MPEG-2transport stream containing numerous channels carried over a single network connection, such as a DS-3 or OC-3 connection. Thus, up to eight program groups are supported by video control shelf 200. This means that each DS-3 connection, for example 118 and 119, carries one program group.

Detailed Description Text - DETX (16):

A program group transported via DS-3 can contain roughly ten channels, while a group transported via OC-3 can contain roughly 35 channels. This indicates a system channel capacity of 80 channels for implementations using DS-3, and a maximum channel capacity of approximately 280 channels for systems implemented using the OC-3 connection. At least one group (and possibly more) will contain

local channels, as illustrated by DS-3 connection 121 and DS-3 connection 123 connecting video control module pair number 8 to SONET add/drop multiplexer 106. The remaining connections comprising, for this preferred embodiment, seven program groups will contain video programming from other sources as illustrated by DS-3connections 118 and 119. Program groups can be multiplexed together to increase overall channel capacity. For example, two half-full DS-3 groups can be combined together, freeing an entire DS-3 for additional programming.

Detailed Description Text - DETX (24):

Turning now to FIG. 9, shown is a schematic view illustrating the architecture of central office 400. Central office 400 receives the combined digital video and data signal over SONET network 150 into SONET add-drop multiplexer 401. SONET add-drop multiplexer 401 exchanges plain old telephone service (POTS) information with PSTN (public switched telephone network) voice switch 409 over connection 408. SONET add-drop multiplexer 401 also exchanges data information over connection 407 with switch 406. SONET add-drop multiplexer 401 communicates video data over connection 402 to video network interface shelf (VNIS) 450. Illustratively, connection 402 is shown as a single connection, however, connection 402 is in reality a plurality of DS-3 communication channels each carrying one program group of the compressed digital video content as described above. VNIS 450 performs a protocol transformation in order to convert the received video data into a standard, compressed digital video transport format, for example but not limited to, digital video broadcast-asynchronous serial interface (DVB-ASI). VNIS 450 is comprised of a plurality of video network interface modules and will be described in detail with reference to FIGS. 10A and 10B.

Detailed Description Text - DETX (27):

Low pass filter shelf 600 communicates POTS information over connection 420 to PSTN voice switch 409, which in turn communicates telephone service over connection 408 through add-drop multiplexer 401 to telco SONET Network 150.

Detailed Description Text - DETX (29):

FIG. 10A is a schematic view illustrating the video network interface shelf 450 of FIG. 9. Central office 400 includes SONET add-drop multiplexer 401 which receives the combined video and data signals from SONET network 150. Central office 400 includes video network interface shelf 450, which includes video network interface module 700 pairs, video output module 750 pair, and shelf processor module 300 pair. Each video network interface module pair includes an active video network interface module 700 and a spare, or stand-by, video network interface module 700. Each video network interface module (VNIM) 700 receives a video program group on DS3 line 402. Each program group is supplied simultaneously to the active VNIM and the stand-by VNIM. Illustratively, each video network interface shelf 450 includes eight pairs of video network interface modules 700, each video network interface module pair receiving the complete program group via a DS3 connection. Each video network interface module pair 700 provides a complete program group to broadcast backplane 1200. Broadcast backplane 1200, the operation of which will be described in detail with reference to FIG. 13, is in communication with video output module pair 750. Video output module pair 750 supplies the program data on connection 404 to video distribution shelf 500 of FIG. 9. The content supplied on connection 404 can be in the form of DVB-ASI content.

Detailed Description Text - DETX (31):

FIG. 10B is a block diagram illustrating the video network interface module 700 of FIG. 10A. The video network interface module 700 receives one program group of digital video programming over redundant DS-3 links 402a and 402b. The DS-3 payload (MPEG-2) data is extracted from the incoming signal and inserted onto broadcast backplane 1200 for delivery to video output module 750. Video network interface module 700 is designed for active/standby redundancy, contains circuitry to allow hotswap, and communicates with the video network

interface shelf processor module 300 for various control purposes. Dual DS-3 signals are presented to each module at the input for link redundancy. Video network interface module 700 includes primary DS-3 line termination and receiver 701a and redundant DS-3 line termination and receiver 701b. The DS-3 line receivers extract the payload data from the incoming bit stream and prepare the content for delivery to the parallel video bus driver 706. Both receivers 701a and 701b are always active, allowing redundancy at the input link. Supervisory module 704 monitors the status of the receivers 701a and 701b over connections 708a and 708b, respectively, and determines which line receiver signal will be used to drive the serial feed to the parallel video bus driver 706. Supervisory module 704 communicates control information to DS-3 line termination and receiver 701a over connection 714a and communicates control information to DS3 line termination and receiver 701bover connection 714b. The parallel video bus driver 706 receives serial data from one of the DS3 line receivers 701a or 701b, over connection 709a or 709b, depending upon which DS-3 line termination and receiver device is active, as determined by the on board supervisory module 704. The serial data is reorganized into the original 8 bit byte format wherein two control data bits are concatenated with the original byte. Differential signaling, and in the preferred embodiment, low voltage differential signaling (LVDS) line drivers (not shown) within parallel video bus driver 706, send this 10-bit "word" to the 20 differential output lines on parallel video bus driver 706 if the supervisory module 704 allows the drivers to be activated.

Detailed Description Text - DETX (35):

FIG. 11B is a block diagram illustrating the video input module 800 of FIG. 11A. Video input module 800 receives all eight program groups in DVB-ASI format over connections 404. The data is converted into LVDS parallel form (with extra control bits added) and made available, via the particular shelf backplane, to all other modules connected to broadcast backplane 1200. Video input module 800 is designed for active/standby redundancy, contains special circuitry to allow hotswap, and communicates with shelf processor module 300 for control purposes. DVB-ASI receiver 801 receives input from eight individual channels 404. Each input line 404 is DVB-ASI compliant. The video data on lines 404 is forwarded from DVB-ASI receiver 801 to LVDS driver module 802 over connection 807. LVDS driver module 802 converts the serial data received from DVB-ASI receiver 801 to parallel form. Special control bits are added to each byte and the data is byte aligned (to be described with reference to FIG. 20).

Detailed Description Text - DETX (36):

When supervisory module 806 asserts the output enable signal on line 808, LVDS drivers for all 160 lines are enabled and all eight program groups are driven onto broadcast backplane 1200 where they are simultaneously made available to all other modules on broadcast backplane 1200.

Detailed Description Text - DETX (39):

Optical receiver 826 converts the optical data stream on connection 836 into an electronic data stream containing the video programming on connection 842. Clock regeneration and data sync 827 regenerates the serial clock from the serial data stream and resynchronizes the data to this clock. A 2.488 GHz clock signal is supplied on connection 844 and the video programming is supplied over connection 843. A 1:16 demultiplexer/receiver and frame detector 828 detects the start of frame bits and demultiplexes the data into 16-bit words. A 155.5 MHz clock signal is supplied over connection 845, the video programming is supplied over connection 846, and frame control information is exchanged with payload extraction device 829 over connection 847. Payload extraction device 829 strips off the framing and overhead bits leaving the video program groups on connection 837. Transmit first-in first-out (FIFO) buffer 831 buffers the eight program groups on connection 837 in a first-in first-out arrangement in order to resynchronize the parallel transmit data rate. LVDS video drivers 832 drive the eight program groups onto broadcast backplane 1200 over connections 838. Illustratively, the optical connection

over which the multiplexed program groups are transported should have sufficient capacity to carry the data such that the program groups may be transported without loss of any information.

Detailed Description Text - DETX (40):

Supervisory module 834 communicates with shelf processor module 300 to set a fault bit over connection 833a, and reads a neighbor fault bit over connection 833b. Supervisory module 834 also enables the LVDS video drivers 832 over connection 839 when appropriate. Voltage management module 841 is responsible for hotswap capability and power management in accordance with that described above.

Detailed Description Text - DETX (42):

Parallel video bus receiver 851 contains LVDS receivers for 160 signals, eight program groups consisting of 20 signals per program group. It receives the video data from the video input module 800 via broadcast backplane 1200. DVB-ASI drivers 856a-856n are responsible for creating a DVB-ASI compliant output on line 501 for each of the program groups. Each connection 857a through 857n includes a serial data stream containing a program group. Each program group is carried on one output connection, therefore each output module contains eight outputs. Any number of DVB-ASI driver modules 856 may exist on a multiple video output module 850, allowing for scalability of the entire system.

Detailed Description Text - DETX (44):

FIG. 11E is a schematic view illustrating a remote video output module of FIG. 11A. Remote video output module 900 outputs a single multiplexed copy of eight 10 bit parallel video program groups along with framing and overhead onto a single fiber optic link for transmission to digital loop carriers (DLCs). A spare module will drive the spare output onto a spare fiber optic link at all times. LVDS video receiver 901 will receive the eight program groups and output a video signal over connection 914 to receive FIFO buffer 904. Since the serial transmit rate and the parallel receive data rate are not equivalent, the eight program groups parallel data is buffered in receive FIFO buffer 904 to resynchronize to the serial data rate. Receive FIFO buffer 904 supplies the video programming over connection 916, supplies FIFO flags over connection 918, and receives FIFO control signals from framer 906 over connection 917.

Detailed Description Text - DETX (54):

LVDS video bus receiver 1009 receives the digital video program groups from broadcast backplane 1200 and converts the differential signals into single-ended signals. The single-ended signals are then sent over connection 1012 to multiplexer 1008. Multiplexer 1008 accepts eight program groups and provides a single program group output on connection 1014 to each subscriber's CO framer 1100. Mux 1008 allows supervisory module 1007 to select the program group that contains the channel selected by a subscriber, and sends that program group to that subscriber's CO framer 1100. The operation of CO framer 1100 will be discussed in detail with reference to FIG. 19. Mux 1008 can simultaneously serve up to n CO framers independently. Supervisory module 1007 writes the desired program group to be selected to a register in CO framer 1100. CO framer 1100 then instructs mux 1008 to select the appropriate program group from the input on connection 1012. CO framer 1100 then selects a single program from the program group and forwards it to DSL transceiver 1001 for transmission to customer premises 1300 over communication channel 16. CO framer 1100 provides the interface to mux 1008. Alternatively, mux 1008 could provide an interface to supervisory module 1007, however, for the preferred embodiment, CO framer 1100 can more conveniently provide the interface to supervisory module 1007. Mux 1008 selects one program group from the eight program groups on connection 1012 and routes the selected program group to the appropriate CO framer 1100. CO framer 1100 then filters the desired program from the program group, combines it with Internet data from bridge 1004 and delivers the combined signal to a customer over communication channel 16.

Essentially, when a user selects a particular channel to view, supervisory module 1007 determines the program group and the packet identifiers (PIDs) within the program group that will extract the chosen channel. Supervisory module 1007 commands mux 1008, via CO framer 1100, to select the appropriate program group, and commands CO framer 1100 to filter certain PIDs. In this manner the chosen program is delivered to the user.

Current US Original Classification - CCOR (1):
370/503

Current US Cross Reference Classification - CCXR (1):
370/498

PGPUB-DOCUMENT-NUMBER: 20030088726

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030088726 A1

TITLE: Serial scaleable bandwidth interconnect bus

PUBLICATION-DATE: May 8, 2003

INVENTOR-INFORMATION: NAME RULE-47	CITY	STATE	COUNTRY
Dillabough, Jeff D.	Belcarra		CA
Tymchuk, Kevin	Vancouver		CA
Gleeson, Maurice	Galway		IE
Oliver, Gordon R.	Belcarra		CA

US-CL-CURRENT: 710/305, 370/252

ABSTRACT:

The serial scaleable bandwidth interconnect (SBI336S) bus provides a 777.6 MHz point-to-point LVDS serial interface that supports a variety of traffic types including support for Fractional links. 8B/10B coding is used on the serial link to provide codes to transmit additional control information across the serial interface. The SBI336S bus encodes ADD BUS clock master timing from the PHY device to the Link Layer device over the DROP BUS. The SBI336S bus can also provide an in-band communication channel between devices.

---------- KWIC ---------

Abstract Paragraph - ABTX (1):

The serial scaleable bandwidth interconnect (SBI336S) bus provides a 777.6 MHz point-to-point LVDS serial interface that supports a variety of traffic types including support for Fractional links. 8B/10B coding is used on the serial link to provide codes to transmit additional control information across the serial interface. The SBI336S bus encodes ADD BUS clock master timing from the PHY device to the Link Layer device over the DROP BUS. The SBI336S bus can also provide an in-band communication channel between devices.

Current US Classification, US Primary Class/Subclass - CCPR (1):

710/305

Current US Classification, US Secondary Class/Subclass - CCSR (1):

370/252

Summary of Invention Paragraph - BSTX (4):

[0002] Typically, an optical fiber, twisted pair electrical or coaxial cable is used for an electrical transmission facility. Such a facility is coupled to a Physical Medium Dependent sublayer (PMD sublayer), which is the lowest sublayer of the two sublayers of the Physical Layer. The Physical Layer (PHY) is the lowest level layer function of the layer functions in the Broadband Integrated Services Digital Network model. The PHY is responsible for typical layer functions, such as bit transfer/reception and bit synchronization. The

prior art discloses a general architecture for connecting a facility to a PHY device and to a Link Layer device. An electrical transmission facility is coupled to a Physical Medium Dependent (PMD) layer device and the latter is coupled through a physical link (PHY-link) interface to the Link Layer device. There is a facility interface on the PMD layer device which may be **SONET/SDH,** DS3 or E3 and which are specified by several National and International standards organizations. The Link Layer device is coupled to the PMD layer device through the PHY-link interface, which consists of an ADD BUS interface that interfaces data flowing from the Link Layer device to the PMD layer device and a DROP BUS interface, which interfaces data flowing from the PMD layer device to the Link Layer device.

Summary of Invention Paragraph - BSTX (8):
[0006] There is also a need for a point-to-point Low Voltage Differential Signaling (**LVDS**) serial PHY-link interface that supports a variety of traffic types and capabilities. There is also a need for a serial bus that is compatible with a 19.44 MHz bus supporting multipoint-multipoint operation over a wide range of channel densities and payload types.

Summary of Invention Paragraph - BSTX (14):
[0011] The Serial Scaleable Bandwidth Interconnect (SBI336S) bus is a 777.6 MHz point-to-point Low Voltage Differential Signaling (**LVDS**) serial PHY-link interface that interconnects PHY devices with Link Layer devices and supports a variety of traffic types including support for Fractional links. The SBI336S bus consists of an ADD BUS interface that receives data from a Link Layer device and directs it to a PHY device. There is also a DROP BUS interface that receives data from a PHY device and directs it to a Link Layer device. 8B/10B coding is used on the serial link to provide codes to transmit additional control information across the serial interface. The SBI336S bus encodes the ADD BUS clock master timing from the PHY device to the Link Layer device over the DROP BUS. The SBI336S bus can optionally provide for an in-band communication channel between devices. This channel is intended for devices at one end of the link to control the device at the other end of the link.

Detail Description Paragraph - DETX (12):
[0038] The term "TVT" refers to Transparent Virtual Tributaries. A TVT1.5 is either a **SONET** VT1.5 Virtual Tributary or a **SDH** TU11 Tributary Unit, which is being multiplexed or demultiplexed from the SBI bus. A TVT2 is either a **SONET** VT2 Virtual Tributary or a **SDH** TU12 Tributary Unit, which is being multiplexed or demultiplexed from the SBI bus.

Detail Description Paragraph - DETX (13):
[0039] This specification describes the SBI, SBI336 and SBI336S, which are PHY-LINK interfaces. The FACILITY interfaces, such as **SONET/SDH,** DS3 or E3, are defined by several National and International standards organizations. Channelized mappings of the PHY, such as M13 for channelization of the DS3 FACILITY, are also defined by several National and International standards organizations.

Detail Description Paragraph - DETX (14):
[0040] The general architecture 50 for connecting a facility 10 to a PHY device 12 and to a Link Layer device 14 is shown as a schematic block diagram in FIG. 1. The facility 10 is coupled to a physical medium dependent layer (PMD) layer device 16 and the PMD layer device 16 is coupled through a PHY-link interface 18 to the Link Layer device 14. There is a facility interface 17 on the PMD layer device 16 which may be **SONET/SDH,** DS3 or E3 and is specified by several National and International standards organizations. The Link Layer device 14 is coupled to the PMD layer device 16 through the PHY-link interface 18 which consists of an ADD BUS interface 20 which interfaces data flowing from the Link Layer device 14 to the PMD layer device 16 and a DROP BUS interface 22 which interfaces data flowing from the PMD layer device 16 to the Link Layer

device 14. This specification describes the PHY-link interface 18 as an SBI, SBI336 or SBI336S bus.

Detail Description Paragraph - DETX (52):
[0078] The SBI multiplexing structure is modeled on the **SONET/SDH** standards.

Detail Description Paragraph - DETX (56):
[0082] The SBI bus uses the **SONET/SDH** virtual tributary structure to carry T1 links, E1 links and TVTs. Unchannelized DS3 and E3 payloads follow a byte synchronous structure modeled on the **SONET/SDH** format.

Detail Description Paragraph - DETX (57):
[0083] The SBI structure uses a locked **SONET/SDH** structure fixing the position of the TU-3 relative to the STS-3/STM-1. The SBI is also of fixed frequency and alignment as determined by the reference clock (REFCLK) and frame indicator signal (C1FP). Frequency deviations are compensated by adjusting the location of the T1/E1/DS3/E3/TVT1.5/TVT2 channels using floating tributaries as determined by the V5 indicator and payload signals (DV5, AV5, DPL and APL) . TVTs also allow for synchronous operation where **SONET/SDH** tributary pointers are carried within the SBI structure in place of the V5 indicator and payload signals (DV5, AV5, DPL and APL). Fractional links use as many bytes as required within a given Synchronous Payload Envelope (SPE) using the payload signals to indicate bytes carrying valid data.

Detail Description Paragraph - DETX (58):
[0084] Table 6 shows the bus structure for carrying T1, E1, TVT1.5, TVT2, DS3, E3 and Fractional tributaries in a **SDH** STM-1-like format. Up to 84 T1s, 63 E1s, 84 TVT1.5s, 63 TVT2s, 3 DS3s, 3 E3s or 3 Fractional links are carried within the octets labeled SPE1, SPE2 and SPE3 in columns 16-270. All other octets are unused and are of fixed position. The frame signal (C1FP) occurs during the octet labeled C1 in Row 1 column 7.

Detail Description Paragraph - DETX (148):
[0170] The SBI336S bus is a 777.6 MHz point-to-point **LVDS** interface that supports the same traffic types and capabilities as the SBI336 bus. 8B/10B coding is used on the serial link to enable data recovery and to provide codes to transmit additional SBI control information across the serial interface. Like the SBI336 bus, the SBI336S bus encodes ADD BUS clock master timing from the PHY device to the Link Layer device over the DROP BUS.

Detail Description Paragraph - DETX (177):
[0199] The in-Band channel includes two bytes of fixed header and a CRC-16 per every 36-byte in-band message. The two-byte header provides control and status between devices at the ends of the **LVDS** link. The CRC-16 is calculated over the entire 34-byte in-band message and provides the terminating end the ability to detect errors in the in-band message. The format of the in-band message and header bytes is shown in Table 33 and Table 34. A description of the header fields is provided in Table 35.

Claims Text - CLTX (10):
9. The interconnect bus according to claim 1, wherein said bus interface device is a **LVDS** interface.

Claims Text - CLTX (21):
20. The apparatus according to claim 12, wherein said bus interface is a **LVDS** interface.

PGPUB-DOCUMENT-NUMBER: 20020001305

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020001305 A1

TITLE: Flexible, self-aligning time and space switch fabrics

PUBLICATION-DATE: January 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
RULE-47			
Hughes, Andrew Milton	Saskatoon		CA
Konkin, Douglas	Saskatoon		CA
McCrosky, Carl Dietz	Saskatoon		CA
Mok, Winston	Vancouver		CA
Roe, Jeffrey Scott	Saskatoon		CA
Sailor, Kenneth Evert	Saskatoon		CA

US-CL-CURRENT: 370/369, 370/442

ABSTRACT:

A time:space:time switch fabric incorporating an odd integer number of spatially distributed data switches and a plurality of spatially distributed data serializers. Each data switch has a first plurality of ingress ports, an equal plurality of egress ports, and a space switch for selectably interconnecting any one of the ingress ports to any one of the egress ports. Each data serializer has an input bus for receiving signals to be routed through the switch fabric, an output bus for outputting signals routed through the switch fabric, a plurality of egress ports selectably connectible to any one of the data switch ingress ports, and an equal plurality of ingress ports selectably connectible to any one of the data switch egress ports. The ingress/egress ports are characterized by:
(A) p planes, where p is a power-of-two integer less than or equal to the number of data serializer ingress and egress ports;
(B) s stages, where s is an odd integer number; and,
(C) a depth d, where d is a power-of-two integer less than or equal to the number of data switch ingress and egress ports.

---------- KWIC ---------

Detail Description Paragraph - DETX (7):

[0047] As previously explained, time and space fabrics must allow all switching stages to recognize and coordinate their switching activities to the boundaries of the grain groups. The present invention uses a special code of 8b/10b to mark the beginnings of STS-1 frame boundaries. The 8b/10b "comma" character is used to mark at least some of the beginnings of STS-1 frames (in the **SONET** J0 octet). This allows the receivers of the TSE and the TBS to recognize STS-1 frame boundaries. The **SONET** frame boundary is used to reset a counter which counts through the repeating 12*9*90 octets of the STS-12 frame. This counter, reduced modulo-twelve, is used to identify the relative positions of the grains of the twelve STS-1s.

Detail Description Paragraph - DETX (8):

[0048] The **8b/10b** "comma" special character is not required to be present in each **SONET** frame; the first occurrence of the comma character sets the frame counter, which then runs modulo-(12*9*90) to count out the positions in successive frames which may or may not contain the comma character.

Detail Description Paragraph - DETX (87):

[0123] Additional considerations applicable to the serial link receivers include use of additional, non-standard **8b/10b** codes to mark both the high-order and low-order **SONET** structure in the TBS and relaxation of the concept of running disparity in **8b/10b** codes to allow the addition of extra **8b/10b** control characters which cause disparity errors in standard **8b/10b** decoders.

Detail Description Paragraph - DETX (93):

[0129] usage of **8b/10b** coding on such serial links to maintain adequate transition density, to detect byte alignment, to detect transmission errors, to identify **SONET** frame boundaries, and to distribute exact framing synchronization through the fabric;

US-PAT-NO: 6480501

DOCUMENT-IDENTIFIER: US 6480501 B1

TITLE: Process for transporting a cell through a switching structure base on a single stage switch

DATE-ISSUED: November 12, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Blanc; Alain	Vence	N/A	N/A	FR
Abbiate; Jean-Claude	La Guade	N/A	N/A	FR

US-CL-CURRENT: 370/422, 370/396 , 370/398

ABSTRACT:

A process for transporting a data cell throughout a switch fabric having a centralized switching structure and a set of distributed, generally remotely located, Switch Core Access Layers (SCAL) permitting the attachment of the protocol adapters. Remotely with respect to the centralized switching structure, the data cell which is received from a telecommunications link is divided into k logical units (LUs) and additional bytes are introduced for permitting the reservation of a bitmap field that will be used for routing through the switch core. Every LU is coded in accordance with the **8B/10B coding** process. Within the centralized switching structure, the k coded LUs are deserialized and the cell clock is obtained for each cell in order to reconstitute the data cell. In addition the routing byte reservations are filled with appropriate values (bit map) for the routing process within the switch by means of an access to an entry routing table. When the cell outputs the switching structure, a second access to a routing table permits the replacement of the previous bit map by new values in order to enhance multicast capabilities. The data cell is divided again in a set of k serialized logical units (LUs) in order to prepare a serialization through k links. The LUs are coded as previously to permit the merging of the LUs when different sets of switches operated in parallel are connected in a port expansion mode. Remotely with respect to the switch core, the coded LUs are deserialized and the data cell is reconstituted by means of the deserialization and extraction of the data cell clock transported by the **8B/10B coding** process. The newly inserted values of the bit map are then used for enhancing multicasting capabilities.

4 Claims, 1 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 1

---------- KWIC ---------

Abstract Text - ABTX (1):

A process for transporting a data cell throughout a switch fabric having a centralized switching structure and a set of distributed, generally remotely located, Switch Core Access Layers (SCAL) permitting the attachment of the protocol adapters. Remotely with respect to the centralized switching structure, the data cell which is received from a telecommunications link is divided into k logical units (LUs) and additional bytes are introduced for permitting the reservation of a bitmap field that will be used for routing

through the switch core. Every LU is coded in accordance with the **8B/10B coding** process. Within the centralized switching structure, the k coded LUs are deserialized and the cell clock is obtained for each cell in order to reconstitute the data cell. In addition the routing byte reservations are filled with appropriate values (bit map) for the routing process within the switch by means of an access to an entry routing table. When the cell outputs the switching structure, a second access to a routing table permits the replacement of the previous bit map by new values in order to enhance multicast capabilities. The data cell is divided again in a set of k serialized logical units (LUs) in order to prepare a serialization through k links. The LUs are coded as previously to permit the merging of the LUs when different sets of switches operated in parallel are connected in a port expansion mode. Remotely with respect to the switch core, the coded LUs are deserialized and the data cell is reconstituted by means of the deserialization and extraction of the data cell clock transported by the **8B/10B coding** process. The newly inserted values of the bit map are then used for enhancing multicasting capabilities.

US-PAT-NO: 6636529

DOCUMENT-IDENTIFIER: US 6636529 B1

TITLE: Semi transparent tributary for synchronous transmission

DATE-ISSUED: October 21, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Goodman; David M	St Albans	N/A	N/A	GB
Brady; Jayne	Belfast	N/A	N/A	GB
Murton; Chris	Chelmsford	N/A	N/A	GB

US-CL-CURRENT: 370/469, 370/466

ABSTRACT:

An interface for converting a variety of incoming digital signals into SDH/SONET format for transmission on a synchronous digital network, by identifying the line code of the incoming digital signal, without identifying the information for OSI layer 2 or 3 processing, i.e. format of each packet. Headers are used to encapsulate incoming packets, and enable packets to be discriminated at the receiver. Advantages of performance monitoring capability and transparency are combined. Identifying line codes enables a greater degree of error detection, than a bit based interface. Also synchronisation can be simpler since line codes for padding can be added or deleted more easily than adding or subtracting bits. The interface is semi-transparent in the sense that identification of line codes limits the interface to those formats that use identifiable line codes, but without limiting to a particular OSI layer 2 or 3 frame format.

19 Claims, 7 Drawing figures

Exemplary Claim Number: 17

Number of Drawing Sheets: 5

---------- KWIC ---------

Detailed Description Text - DETX (14):

Mapping of one rate or format into another is well known. Bellcore TR-0253 describes in detail the standard mappings of the common asynchronous transmission formats (DS0, DS1, DS2, DS3, etc) into **SONET**. Similar mappings are defined for the ETSI hierarchy mapping into SDH. Optical transmission equipment has mapped one proprietary format into another. For example, FD-565 could carry Nortel's FD-135 proprietary format as well as the DS3 standard format. However, the standards or proprietary schemes allow transportation of a very specific set of signals, with format specific hardware. These methods of mapping cannot be used to map rates that vary significantly from the standard. Furthermore, these mappings are each precisely tuned for a particular format and a particular bit-rate, with e.g. a .+-.20 ppm tolerance. If a signal has, for example, a bit rate even 1% different than that of a DS3, cannot be transported within **SONET**. In addition, a different hardware unit is generally required to perform the mapping of each kind of signal. A line **coding such as 8B/10B** or 4B/5B may be used and produces a format with a higher rate than the original signal.

PGPUB-DOCUMENT-NUMBER: 20010014104

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010014104 A1

TITLE: 10 Gigabit ethernet mappings for a common LAN/WAN PMD interface with a simple universal physical medium dependent interface

PUBLICATION-DATE: August 16, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
RULE-47			
Bottorff, Paul A.	Palo Alto	CA	US
Figueira, Norival R.	San Jose	CA	US
Martin, David W.	Stittsville		CA
Armstrong, Timothy J.	Stittsville		CA
Raahemi, Bijan	Nepean		CA

US-CL-CURRENT: 370/471, 370/419 , 370/474 , 370/477 , 370/537 , 370/543

ABSTRACT:

An Ethernet mapping enables high speed Ethernet data streams having a data rate of 10 Gb/s to be transported across a synchronous packet switched network fabric having a standard SONET OC-192 line rate of 9.953280 Gbaud. The 10 Gb/s Ethernet data stream is compressed by removing interframe gaps between successive MAC frames to produce a compressed data stream, which is then mapped to a synchronous container. The synchronous container is then launched across the synchronous packet switched network fabric at a standard SONET OC-192 line rate of 9.953280 Gbaud. The synchronous container is preferably provided as a stripped STS-192c frame having only A1 and A2 octets of the Transport Overhead (TOH). The compressed data stream is mapped directly to the synchronous container, starting at the first octet following the A1 and A2 octets, without first being inserted into a conventional STS-192c SPE, so that most of the space normally used for TOH and Path overhead (POH) within a conventional STS-192c frame is freed-up for carrying the compressed data stream. At a receiving interface, the compressed data stream is extracted from received synchronous containers and decompressed, by insertion of interframe gaps between successive MAC frames, to generate a recovered 10 Gb/s Ethernet data stream. The starting bit of each successive MAC frame can be identified by examination of the length field of the immediately previous MAC frame.

---------- KWIC ---------

Detail Description Paragraph - DETX (8):

[0034] FIG. 2 schematically shows a prior art physical layer interface for coupling high speed Ethernet traffic to a **SONET**/SDH packet switched network medium 4. As shown in FIG. 2, the conventional PCS 10 and PMA 12 are grouped together as a combined PCS/PMA HARI 30 which mediates data transport between the (conventional) data link layer 8 and a modified PMD sub-layer 14a. The HARI 30 exchanges data with the modified PMD 14a using 4 parallel data channels (in each direction) operating at a line rate of 3.125 Gbaud. The modified PMD 14a is subdivided into **8B/10B** and 64/66 encoding layers 32,34; a framer FIFO 36; a scrambler 38; and a conventional electron/optical conversion layer 40.

Thus in the prior art device of FIG. 2, much of the data encoding, framing, and scrambling functionality conventionally performed in the PCS 10 and PMA 12 are relocated into the PMD 14a. The PMD 14a is designed to operate in one of two modes depending on the LAN/WAN configuration of the network (see FIG. 7). In particular, in a LAN configuration, this interface is intended to achieve a data rate in the data link layer 8 of 10 Gb/s, in conformance with the high speed Ethernet standard. In order to obtain this data rate, the framer FIFO 36, scrambler 38 and converter 40 of the PMD 14a (and medium 4) is operated at a line rate of 10.3125 Gbaud. This line rate is significantly higher than that supported by the SONET/SDH standard, which precludes the use of conventional (and legacy) SONET/SDH routing systems within the network medium 4.

Detail Description Paragraph - DETX (23):

[0049] In an alternative embodiment, a conventional 16 bit low voltage differential signal (LVDS) chip interface can be used between the physical medium dependent layer 46 and the physical medium attachment layer 44.

US-PAT-NO: 6654565

DOCUMENT-IDENTIFIER: US 6654565 B2

TITLE: System and method for increasing upstream communication efficiency in an optical network

DATE-ISSUED: November 25, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kenny; John J.	Suwanee	GA	N/A	N/A

US-CL-CURRENT: 398/182, 372/38.02 , 372/38.04 , 372/38.07

ABSTRACT:

An optical transmitter of a subscriber optical interface and an optical receiver of a laser transceiver node can be designed to a frequency of data that is formatted according to a predetermined network protocol, that is encoded with a predetermined coding scheme, and that is transmitted according to a predetermined data transmit timing scheme. The frequency of data is an occupied frequency of a protocol when the data comprises a maximum number of like bits permitted by the protocol. An optical transmitter and optical receiver can be designed to a lowest occupied frequency of data that is encoded with 8B/10B encoding, and that is propagated upstream according to time division multiple access (TDMA). In this way, upstream optical communications can be maximized for speed.

11 Claims, 21 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 11

---------- KWIC ---------

Brief Summary Text - BSTX (24):

For each high frequency circuit mentioned above, adjusting of the time constant can comprise adjusting capacitance values to correspond to the frequency of data propagated according to the predetermined network protocol comprising Gigabit Ethernet with **8B/10B** encoding and a predetermined timing scheme such as TDMA, according to one exemplary embodiment. This usually means that the high pass time constants of each high frequency circuit can be set lower than time constants designed to handle data formatted according to different conventional protocols such as **SONET**.

Detailed Description Text - DETX (81):

At the exemplary speed of half gigabit per second data rate, the minimum frequency of a **SONET** signal is approximately lower than 4.3 MHz, and for Ethernet with **8B/10B** encoding, is approximately 52 MHz. Suitable time constants for **SONET** signals at this data rate are approximately a minimum of 184 nanoseconds, and for Gigabit Ethernet are approximately 15 nanoseconds. Both are based on a time constant corresponding to approximately five times the minimum occupied frequency.

Detailed Description Text - DETX (83):

Meanwhile, the dashed slanted line 810 represents the starting and lowest frequency for data formatted according to a network protocol encoded with a predetermined coding scheme. According to one exemplary aspect of the present invention, the inventors of the present application have discovered that the network protocol comprising Gigabit Ethernet having a predetermined encoding scheme such as **8B/10B** encoding does not extend to as low an occupied frequency as that of data formatted according to conventional optical network protocols such as **SONET**.

Detailed Description Text - DETX (112):
Specifically, the predetermined network protocol can comprise half Gigabit or faster Ethernet encoded with **8B/10B** encoding and transmitted according to time division multiple access (TDMA). Those skilled in the art recognize that a significant portion of optical equipment on the market as of the filing date of this specification is designed to operate with a **SONET** standard optical network protocol.

Detailed Description Text - DETX (115):
Dashed line 810 illustrates the lowest frequency that can be occupied by the network protocol of the present invention as well as the predetermined coding scheme. The inventors have discovered that Gigabit Ethernet protocol with **8B/10B** encoding has a different lowest frequency relative the lowest frequency of a conventional network protocol such as **SONET**. The time constants of the present invention are adjusted to quickly achieve this lowest frequency of the network protocol of the present invention, which can comprise Gigabit Ethernet with **8B/10B** encoding.

Detailed Description Text - DETX (118):
Opposite to the conventional network protocol of **SONET,** the network protocol of the present invention that is encoded with a predetermined coding scheme, helps limit the number of consecutive ones and zeros between any two code groups of a data string. According to one exemplary embodiment of the present invention, the coding scheme comprises **8B/10B** encoding.

Detailed Description Text - DETX (162):
Next, in step 1510 a first time constant of a first high pass filter circuit 1000 is adjusted to correspond with the frequency of the data encoded according to the network protocol and with the predetermined encoding scheme. As noted above, the inventors have discovered that the exemplary network protocol of Gigabit Ethernet with the predetermined encoding scheme of **8B/10B** encoding has a lowest occupied frequency that is higher than the lowest occupied frequency of conventional optical network protocols such as **SONET**.

Detailed Description Text - DETX (180):
The predetermined network protocol comprising Gigabit Ethernet and the predetermined encoding scheme comprising **8B/10B** encoding allows the present invention to increase the transmission speed of upstream optical communications when a predetermined timing scheme such as time division multiple access is used in the optical network. As mentioned above, Gigabit Ethernet with **8B/10B** encoding comprises a higher minimum occupied frequency for a given transmission rate compared to that of other conventional optical network protocols such as **SONET**. With the higher minimum occupied frequency, this allows a transmitter and a receiver to be constructed with lower time constants and resulting in significantly increased speed in transitioning from one transmitter to another when a predetermined timing scheme such as TDMA is employed by the upstream optical communications.

Mok et al
same inventors
related
PPB

PGPUB-DOCUMENT-NUMBER: 20020114348

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020114348 A1

TITLE: Bus interface for transfer of multiple SONET/SDH rates over a serial backplane

PUBLICATION-DATE: August 22, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
RULE-47			
McCrosky, Carl D.	Saskatoon		CA
Guay, Bernard	Vancouver		CA
Konkin, Doug	Saskatoon		CA
Lang, Steven F.	Vancouver		CA
Mok, Winston K.	Vancouver		CA

US-CL-CURRENT: 370/465, 370/389

ABSTRACT:

A bus interface for transfer of SONET/SDH data that supports a plurality of SONET/SDH flows. The invention supports two line coding schemes: 8B/10B encoding of STS-12, and SONET scrambled coding for STS-12, STS-48, and STS-51. The invention additionally supports two modes of line testing: entire links can be tested by inserting and checking PRBS sequences, and the SPE payload of the largest concatenated STS-Nc which the link can carry (STS-12c, STS-48c, STS-51c) can be individually tested by inserting and checking PRBS sequences.

---------- KWIC ---------

Summary of Invention Paragraph - BSTX (11):
[0009] It is a further object of this invention to support two line coding schemes: **8B/10B** encoding of STS-12 at 622.08 Mb/s producing an effective line rate of 777.6 Mb/s, and **SONET** scrambled coding for all three rates (STS-12, STS-48, and STS-51) with no expansion in effective line rates.

Summary of Invention Paragraph - BSTX (16):
[0013] The bus interface of the present invention supports the following **SONET**/SDH flows: an **8B/10B** solution for STS-12 (777.6 Mb/s), and scrambled **SONET**/SDH for STS-12 (622.08 Mb/s), STS-48 (2488.32 Mb/s), and STS-51 (2643.84 Mb/s). Each such **SONET**/SDH flow can be transmitted in duplex over a single pair of differential traces in each direction. The differential signaling techniques used may be based on LVDS-like electrical parameters and the power consumed by the implementation should be minimized. The bus interface includes options for manipulation of **SONET**/SDH Section, Line, and Path overhead octets, and additionally supports line testing via PRBS techniques.

Summary of Invention Paragraph - BSTX (18):
[0015] The bus interface of the present invention comprises a transmitter module and a receiver module. The transmitter module either **8B/10B** encodes or S-NRZ scrambles before serializing and transmitting the **SONET**/SDH frames. The

370/476

10/080,485

AU2665

Ex Hung Vu

receiver recovers bit boundaries then either uses 8B/10B coding to find byte alignment and 8B/10B control characters to find SONET framing, or uses SONET/SDH A1/A2 frame delineation to find both byte and frame boundaries.

Summary of Invention Paragraph - BSTX (19):
[0016] The 8B/10B control characters labeling the SONET/SDH frame boundaries are decoded into SONET/SDH control signals.

Summary of Invention Paragraph - BSTX (20):
[0017] By mapping a descrambled SONET/SDH data stream into 8B/10B control characters, proper data transitions on serial links can be ensured. Also, the mapping preserves the DC balance.

Summary of Invention Paragraph - BSTX (22):
[0019] Alternatively, the signal may be scrambled using standard SONET/SDH scrambling with the x.sup.7+x.sup.6+1 scrambling polynomial. This option avoids expanding the required serial link bandwidth (8B/10B requires 10/8=1.25 times the basic SONET/SDH bandwidth). This advantage translates into lower power consumption and greater reach for a lower frequency signal. However, the scrambling option does introduce the possibility that the scrambler will generate a sufficiently long sequence of unchanging bits that the LVDS links will lose bit alignment. The underlying LVDS technology is tolerant of transitionless runs of up to 80 bits. This drives the probability of loss of bit alignment to acceptably low levels.

Detail Description Paragraph - DETX (6):
[0031] The TSEC block 30, 32, 34 converts the internal data representation to the selected external serial transmission format. If configured for emission of scrambled data, the TSEC applies SONET/SDH scrambling to the data stream. The scrambling is accomplished with the x.sup.7+x.sup.6+1 scrambling polynomial applied to all SONET/SDH octets other than A1, A2, and J0/Z0. This scrambler restarts each SONET/SDH frame. Alternately, the TSEC can be configured for the emission of a Serial TelecomBus datastream in which the datastream is encoded using the 8B/10B based Serial TelecomBus format.

Detail Description Paragraph - DETX (47):
[0072] The Receive SONET Data Framer (RSEF) blocks 66, 68, 72 frame to the receive stream to find 8B/10B character boundaries. They also contain a FIFO to bridge between the timing domain of the RSEF links and the system clock timing domain.

Detail Description Paragraph - DETX (50):
[0075] In Serial TelecomBus mode, the RSEF recovers character alignment by searching for the 8B/10B K28.5 frame alignment control character, which is used to identify the J0 position of the SONET/SDH frame. When the RSEF is out of character alignment, it is also necessarily out of frame alignment. When the RSEF is out of character alignment, the first K28.5 character found will determine the character alignment and transition the RSEF into the character alignment state. A count of line code violations (LCVs), either unrecognized 8B/10B characters or incorrect disparity characters, is maintained. If the number of LCVs within a window of 15 received characters exceeds a threshold of 4, frame and character alignment is lost and the block attempts to reframe on the next J0 character. To find frame alignment, the RSEF must locate two K28.5 characters at the correct position with respect to each other, separated by 9720 bytes, regardless of whether the RSEF is currently character aligned or not. To go out of frame, the RSEF must either go out of character alignment or encounter four instances of K28.5 characters not in the J0 position of the current frame alignment and uninterrupted by an instance of a J0 being in the correct position.

Detail Description Paragraph - DETX (65):

[0090] The Character Aligner 114 locates character boundaries in the incoming 8B/10B data stream. The framer logic may be in one of two states, SYNC state and HUNT state. It uses the 8B/10B control character (K28.5) used to encode the SONET/SDH J0 byte to locate character boundaries and to enter the SYNC state. It monitors the receive data stream for line code violations (LCV). An LCV is declared when the running disparity of the receive data is not consistent with the previous character or the data is not one of the characters defined in IEEE std. 802.3. Excessive LCVs are used to transition the framer logic to the HUNT state.

Detail Description Paragraph - DETX (92):

[0117] The preferred embodiment provides a new use of 8B/10B control characters to label SONET/SDH transport frame, high-order path frame, and low-order path frame boundaries. The types of bytes that are encoded in 8B/10B control characters are configurable to suit different classes of SONET/SDH equipment (multiplex section terminators, high-order path terminators and low-order path terminators).

Detail Description Paragraph - DETX (93):

[0118] Furthermore, the use of 8B/10B encoding on de-scrambled SONET/SDH data streams in order ensures data transitions on the serial links and preserves DC balance.

Detail Description Paragraph - DETX (99):

[0124] In S-NRZ mode, the same mechanism for frame alignment in a multi-device environment applies, but frame alignment is found by SONET/SDH A1/A2 alignment instead of by 8B/10B codes. Once frame alignment is found, the receiver FIFO is managed in the identical manner.

Claims Text - CLTX (2):

1. An interface device for connecting SONET/SDH termination devices with payload processing devices, comprising: (a) a receive module operative to receive incoming SONET/SDH signal streams, to recover bit boundaries, and to recover byte and frame alignment by one of using SONET/SDH A1/A2 frame delineation to find both byte and frame boundaries and using 8B/10B coding to find byte boundaries and 8B/10B control characters to find frame boundaries; and (b) a transmit module operative to scramble STS-48 and STS-51, to one of 8B/10B encode and scramble STS-12, to serialize said SONET/SDH signal streams, convert said SONET/SDH signal streams into outgoing low voltage differential signal (LVDS) levels, and to transmit said SONET/SDH signal streams.